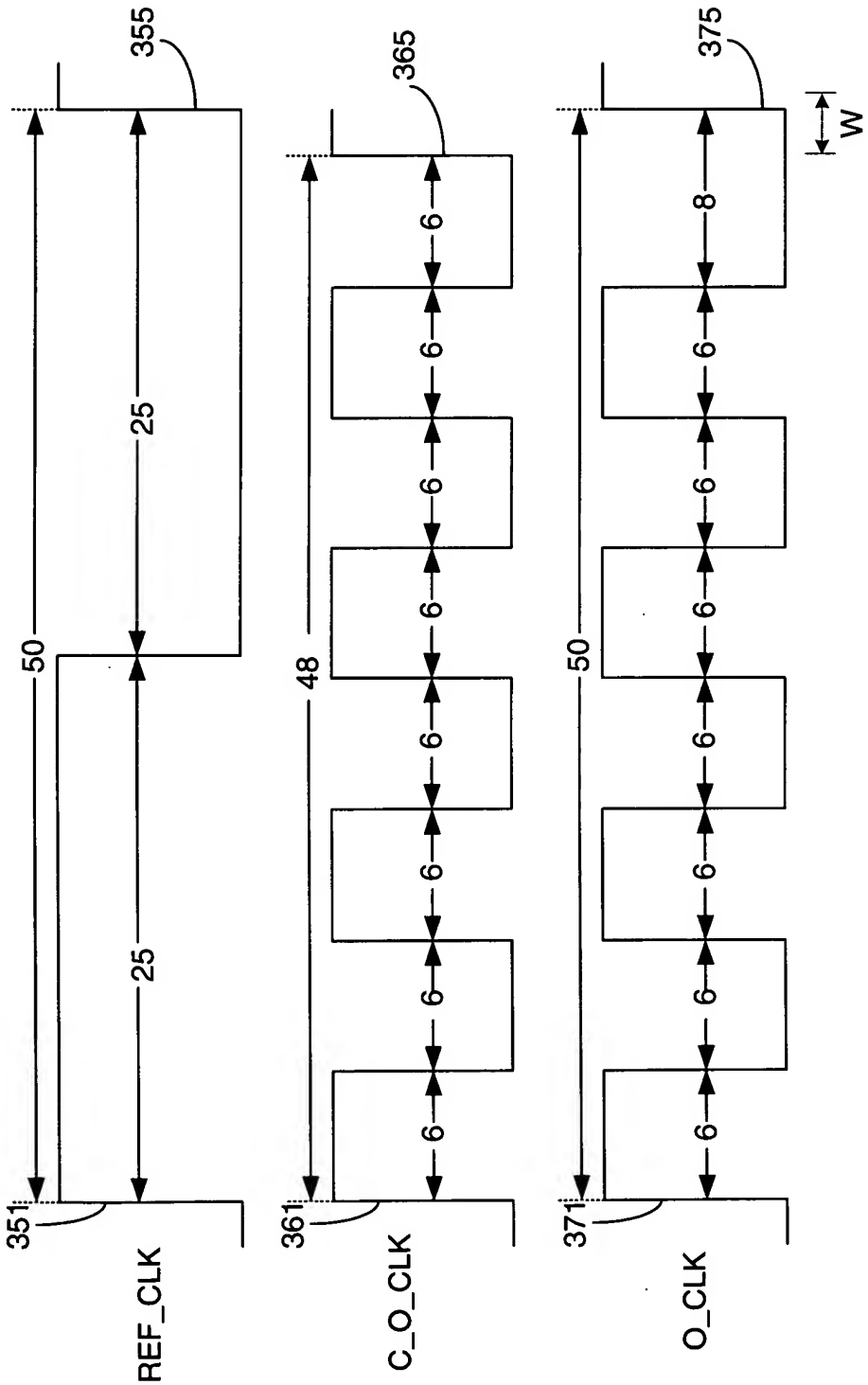


**FIG. 1**
**Prior Art**

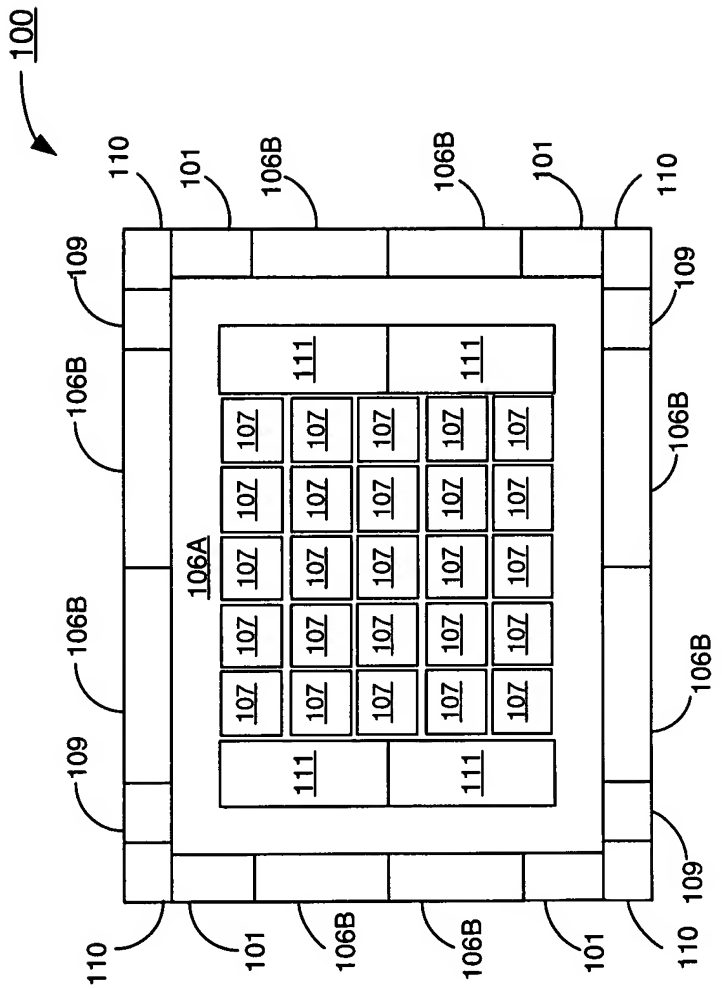
100
110
101
106B
106B
101
110
109
109
106B
106B
106A
111
111
107
111
111
109
109
110
101
106B
106B
101
110

FIG. 2

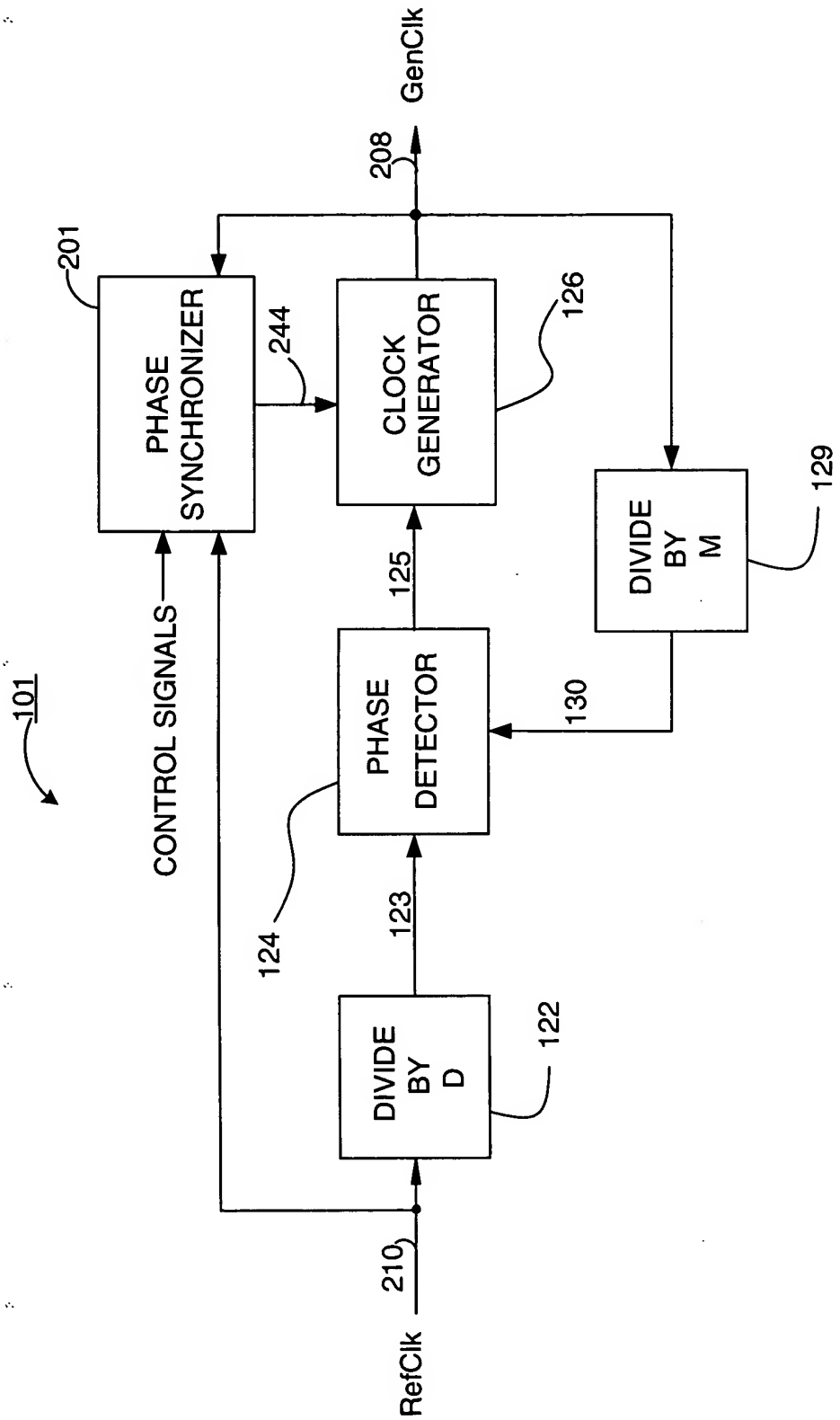
101
CONTROL SIGNALS
201
PHASE SYNCHRONIZER
244
CLOCK GENERATOR
126
208
GenClk
DIVIDE BY M
129
130
PHASE DETECTOR
125
124
123
DIVIDE BY D
122
210
RefClk

FIG. 3

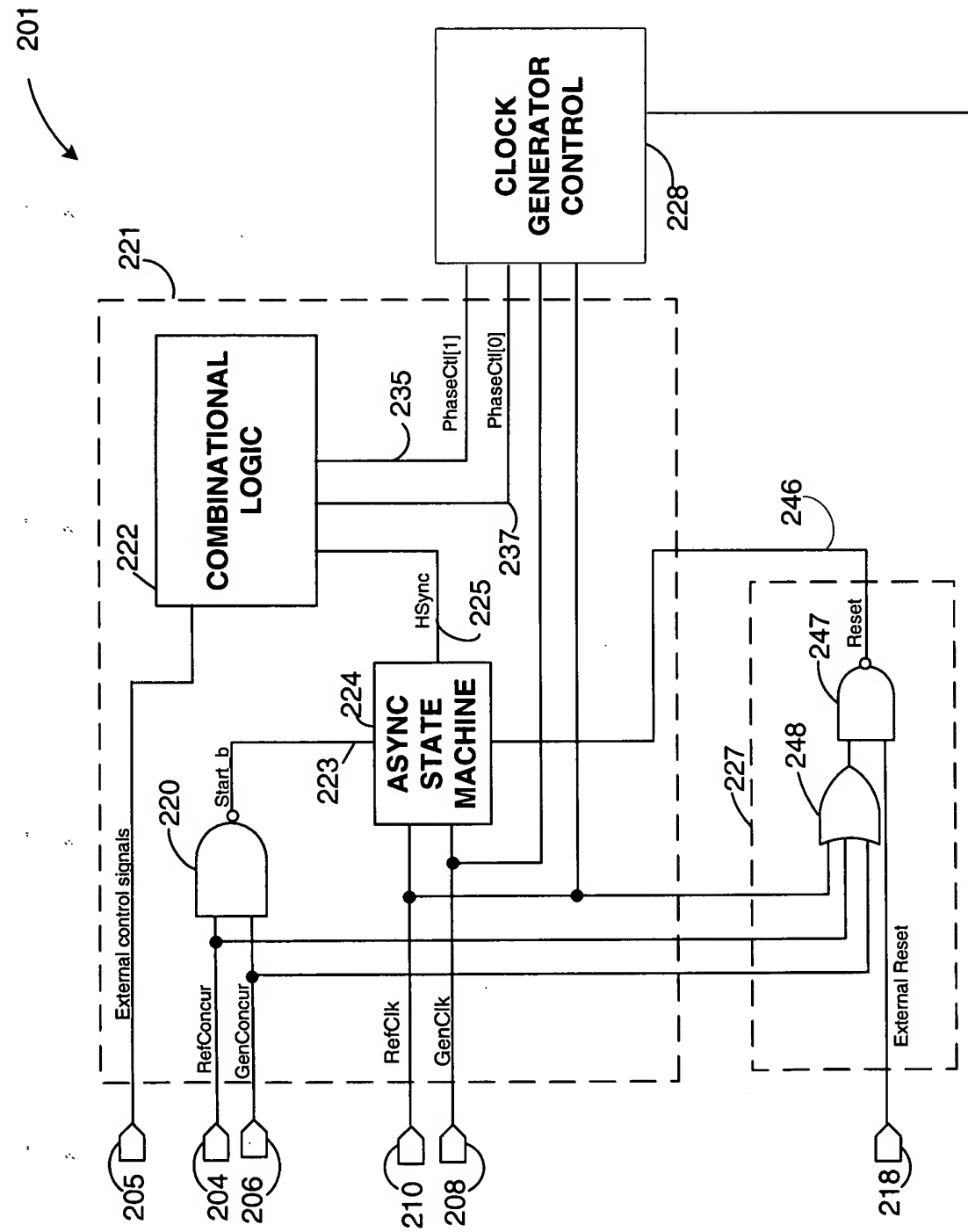
201
221
CLOCK GENERATOR CONTROL
228
To ClkGen
244
COMBINATIONAL LOGIC
222
235
PhaseCtl[1]
PhaseCtl[0]
237
246
HSync
225
ASYNC STATE MACHINE
224
223
247
Reset
248
227
220
Start_b
External control signals
RefConcur
GenConcur
RefClk
GenClk
External Reset
205
204
206
210
208
218

FIG. 4

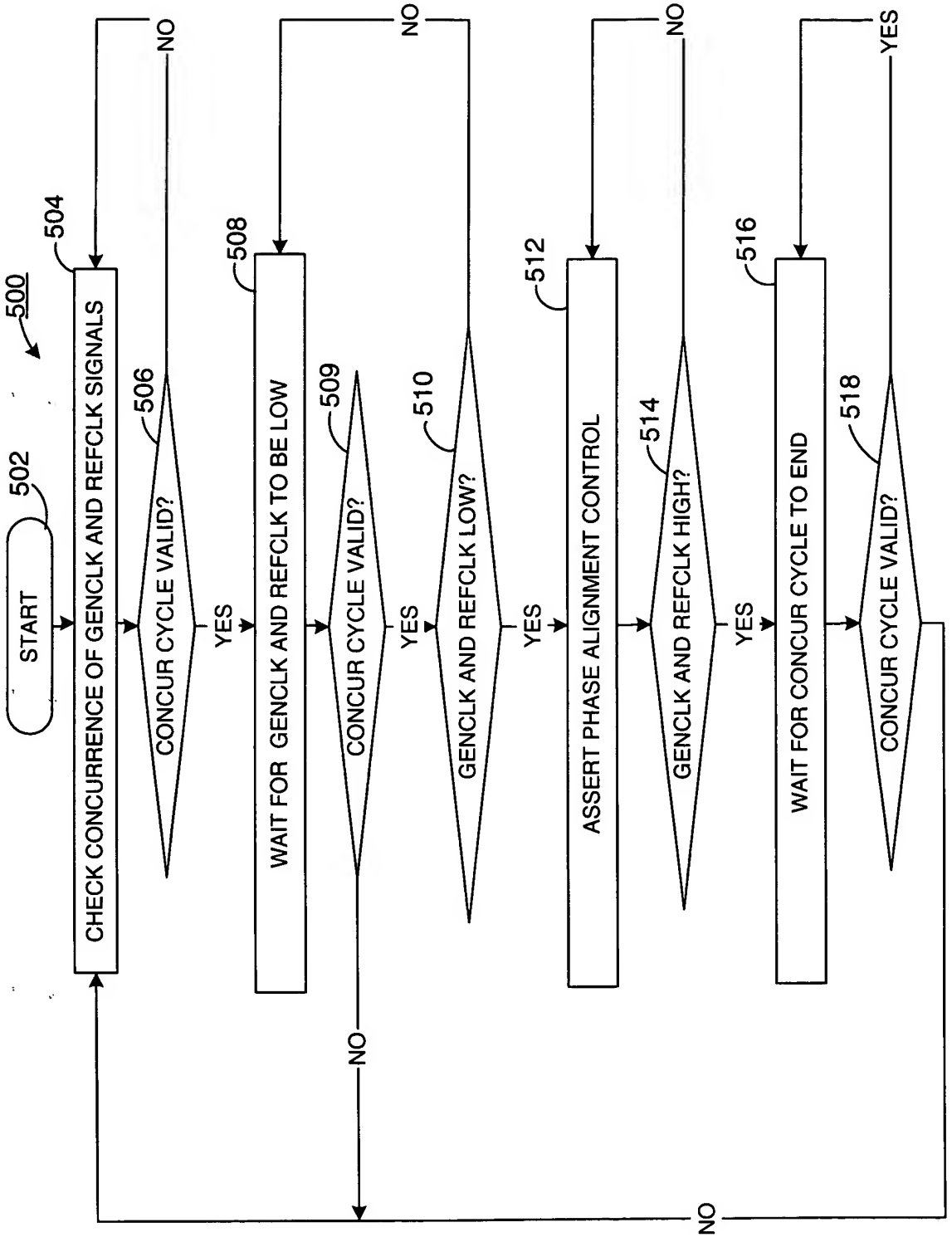
500
START
502
CHECK CONCURRENCE OF GENCLK AND REFCLK SIGNALS
504
CONCUR CYCLE VALID?
506
NO
YES
WAIT FOR GENCLK AND REFCLK TO BE LOW
508
CONCUR CYCLE VALID?
509
NO
YES
GENCLK AND REFCLK LOW?
510
NO
YES
ASSERT PHASE ALIGNMENT CONTROL
512
GENCLK AND REFCLK HIGH?
514
NO
YES
WAIT FOR CONCUR CYCLE TO END
516
CONCUR CYCLE VALID?
518
YES
NO

FIG. 5

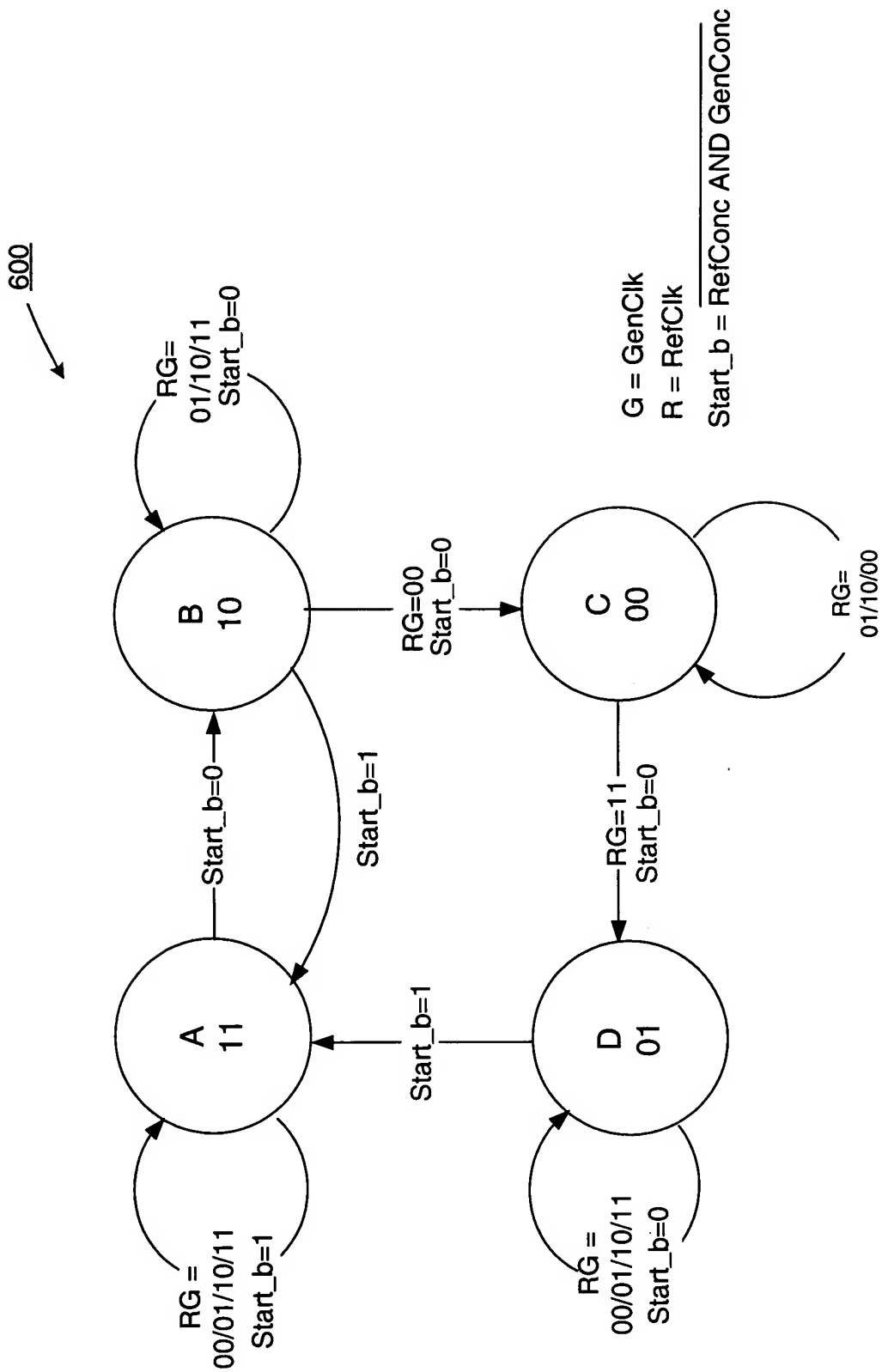
600
A
11
B
10
C
00
D
01
RG =
00/01/10/11
Start_b=1
RG=
01/10/11
Start_b=0
RG=
01/10/00
RG =
00/01/10/11
Start_b=0
Start_b=0
Start_b=1
RG=00
Start_b=0
RG=11
Start_b=0
Start_b=1
G = GenClk
R = RefClk
Start_b = RefConc AND GenConc

FIG. 6

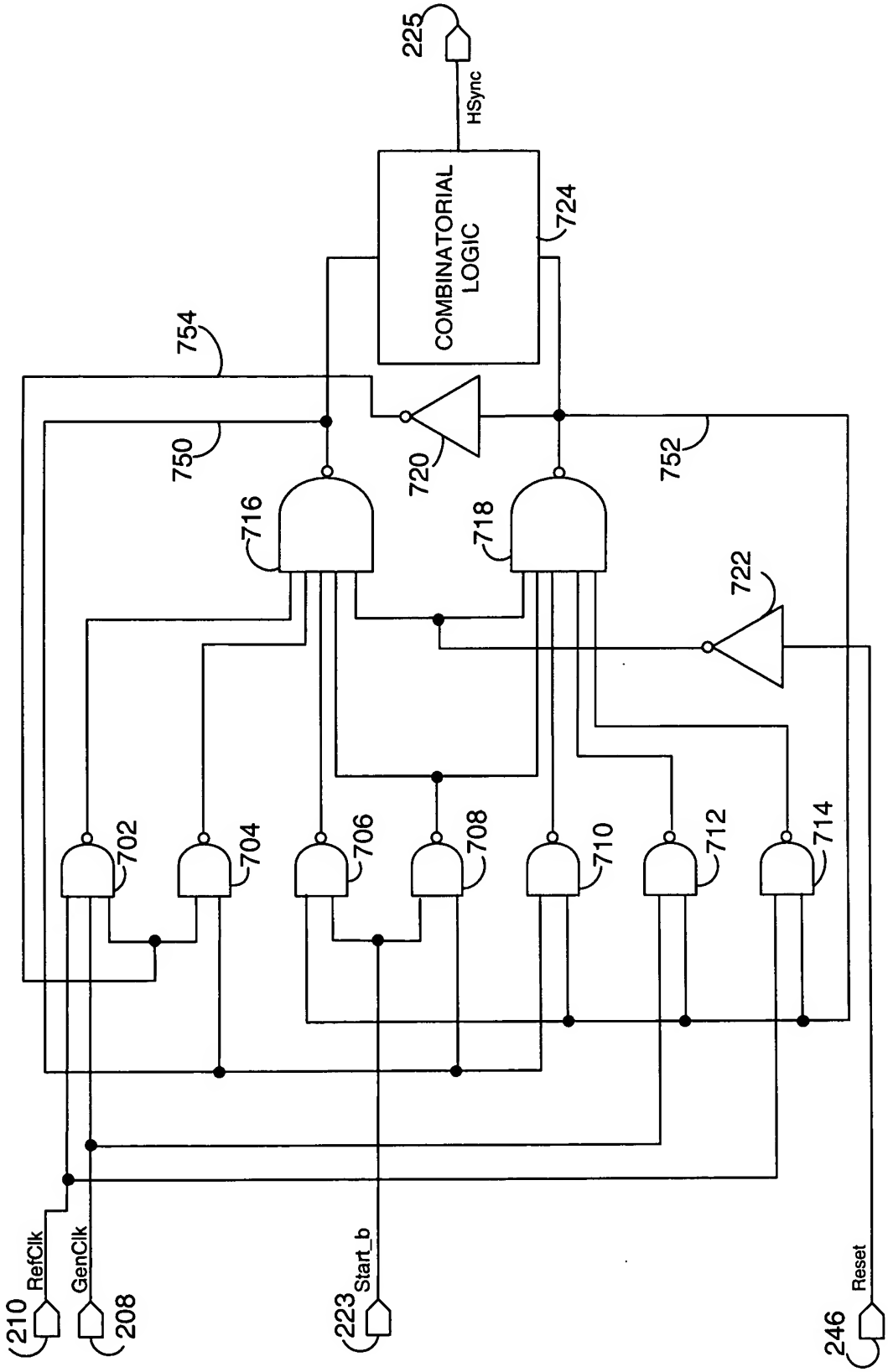
700
225
HSync
COMBINATORIAL LOGIC
724
754
750
720
752
716
718
722
702
704
706
708
710
712
714
210
RefClk
208
GenClk
223
Start_b
246
Reset

FIG. 7

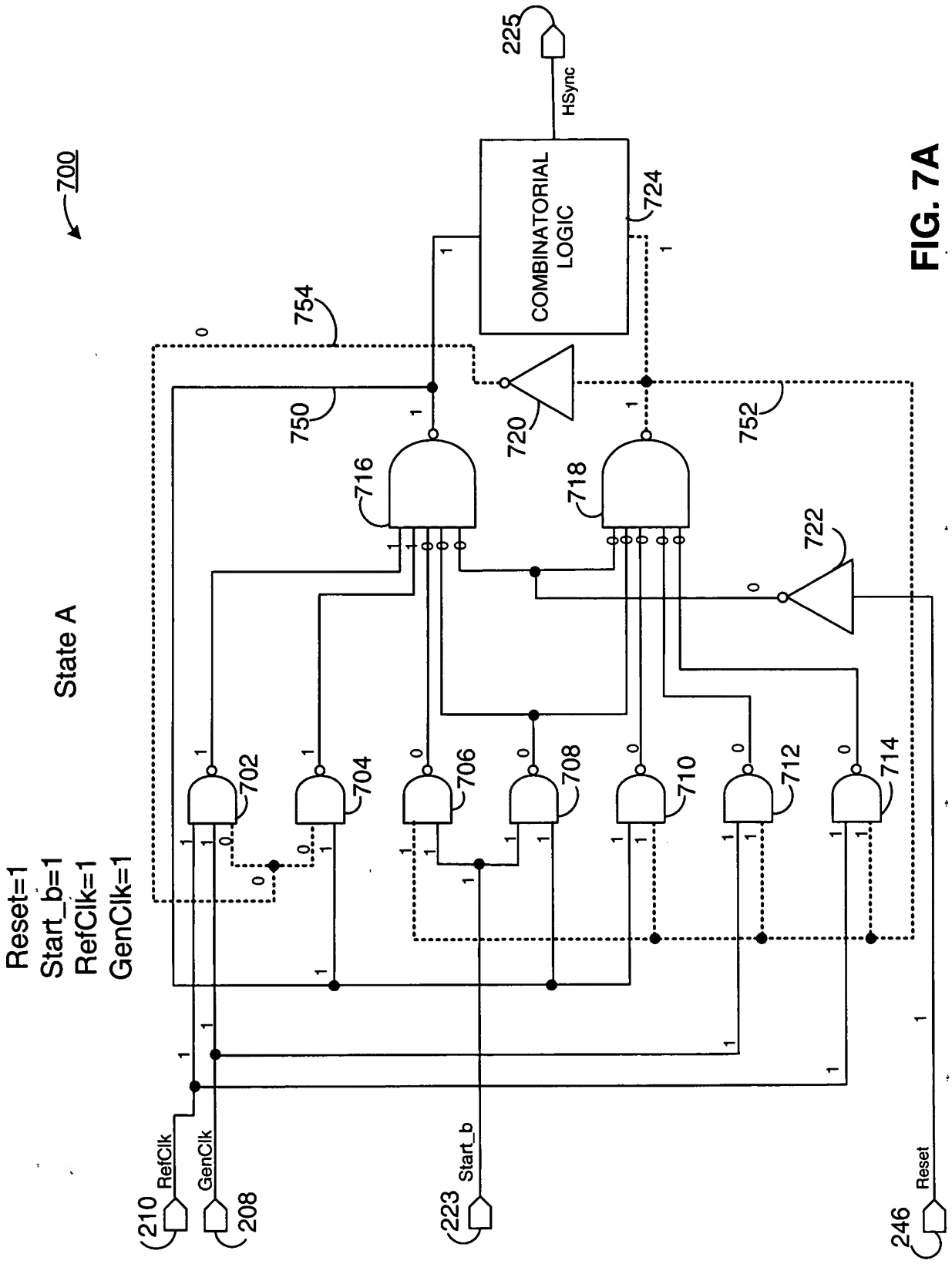
700
State A
Reset=1
Start_b=1
RefClk=1
GenClk=1
COMBINATORIAL LOGIC
HSync
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
RefClk
GenClk
Start_b
Reset
210
208
223
246

FIG. 7A

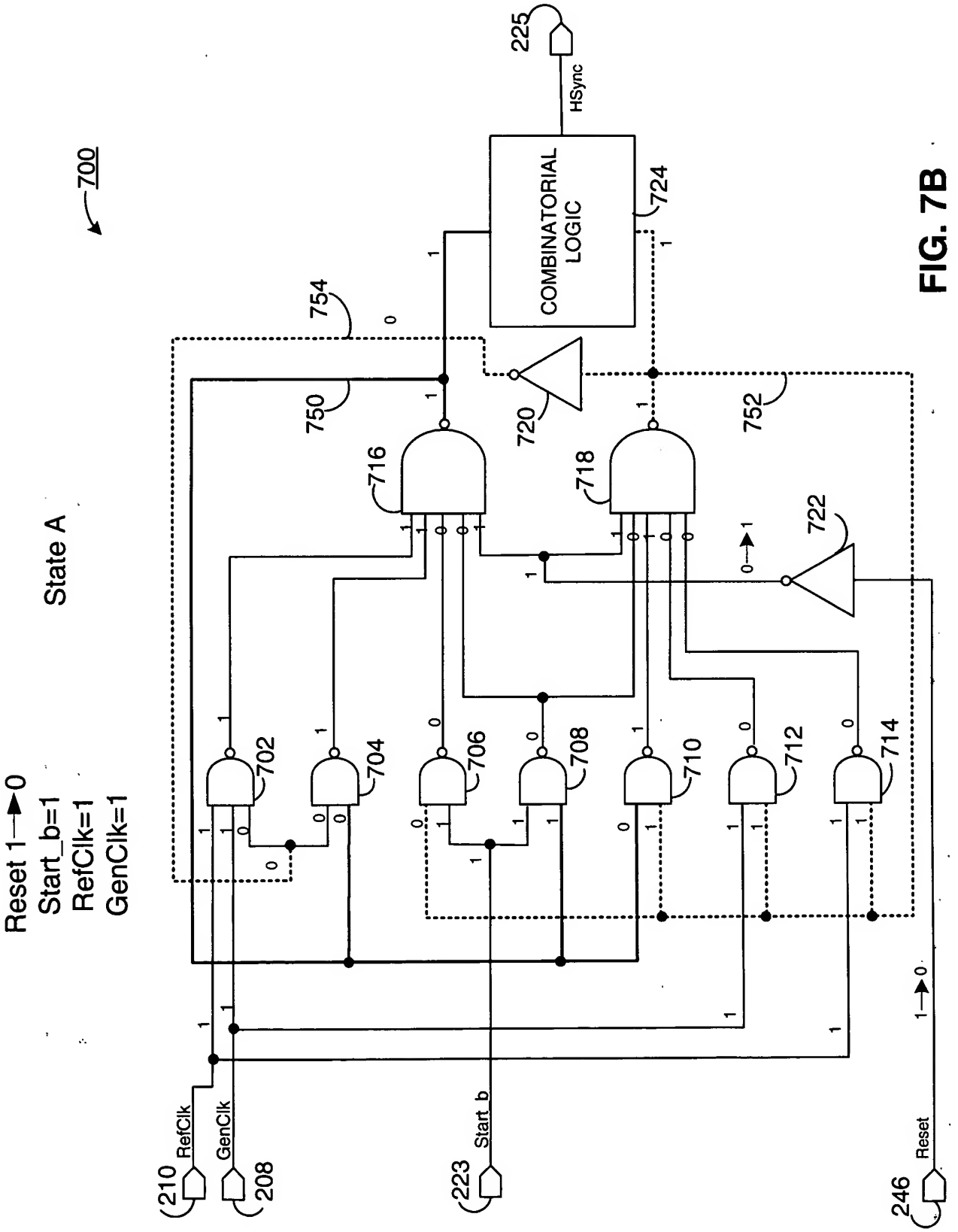
700
State A
Reset 1→0
Start_b=1
RefClk=1
GenClk=1
RefClk
GenClk
Start_b
Reset
HSync
COMBINATORIAL LOGIC
210
208
223
246
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714

FIG. 7B

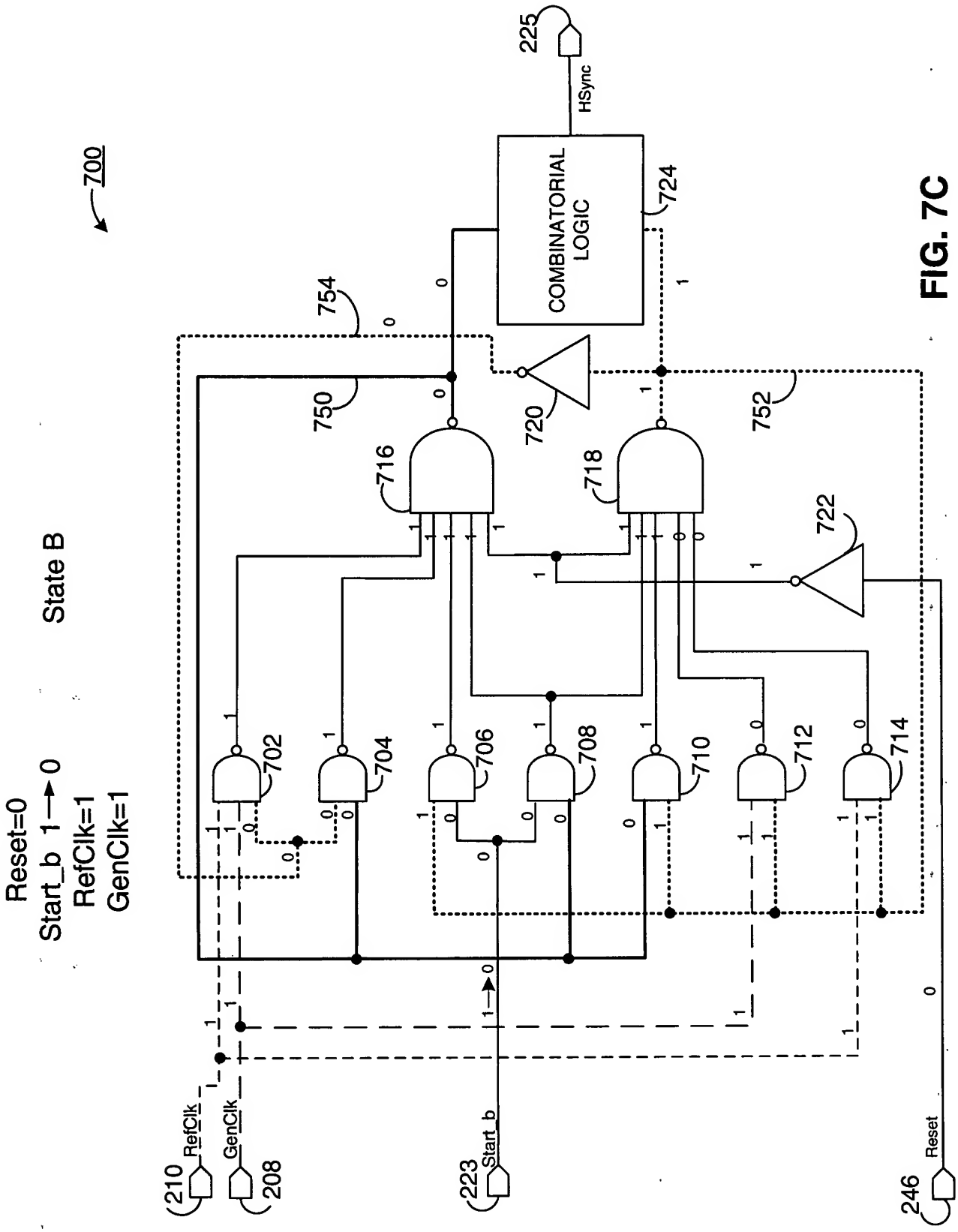
700
Reset=0
Start_b 1→0
RefClk=1
GenClk=1
State B
225
HSync
COMBINATORIAL LOGIC
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
210
RefClk
208
GenClk
223
Start_b
246
Reset

FIG. 7C

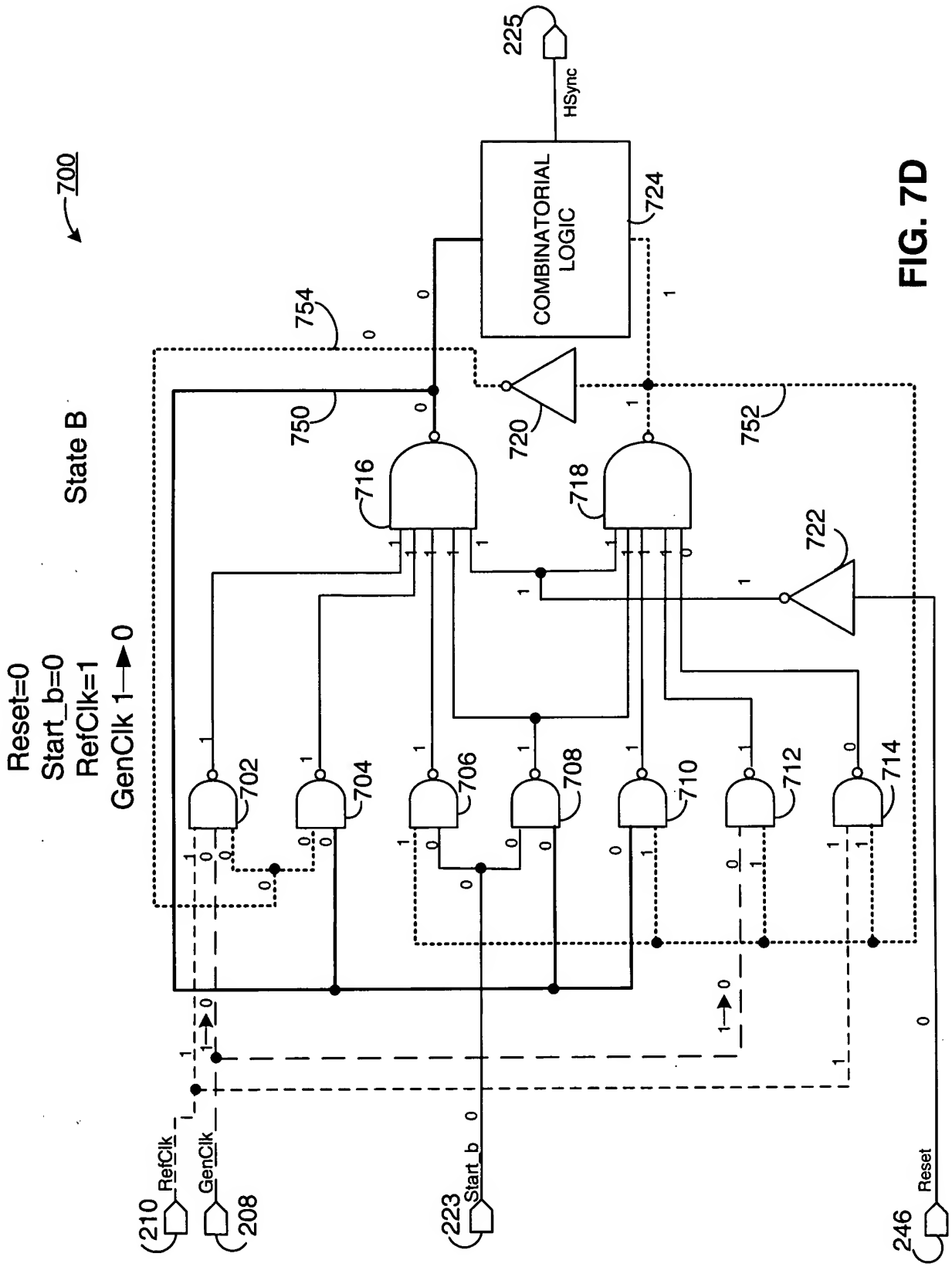
700
Reset=0
Start_b=0
RefClk=1
GenClk 1→0
State B
COMBINATORIAL LOGIC
HSync
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
210
RefClk
208
GenClk
223
Start_b
246
Reset

FIG. 7D

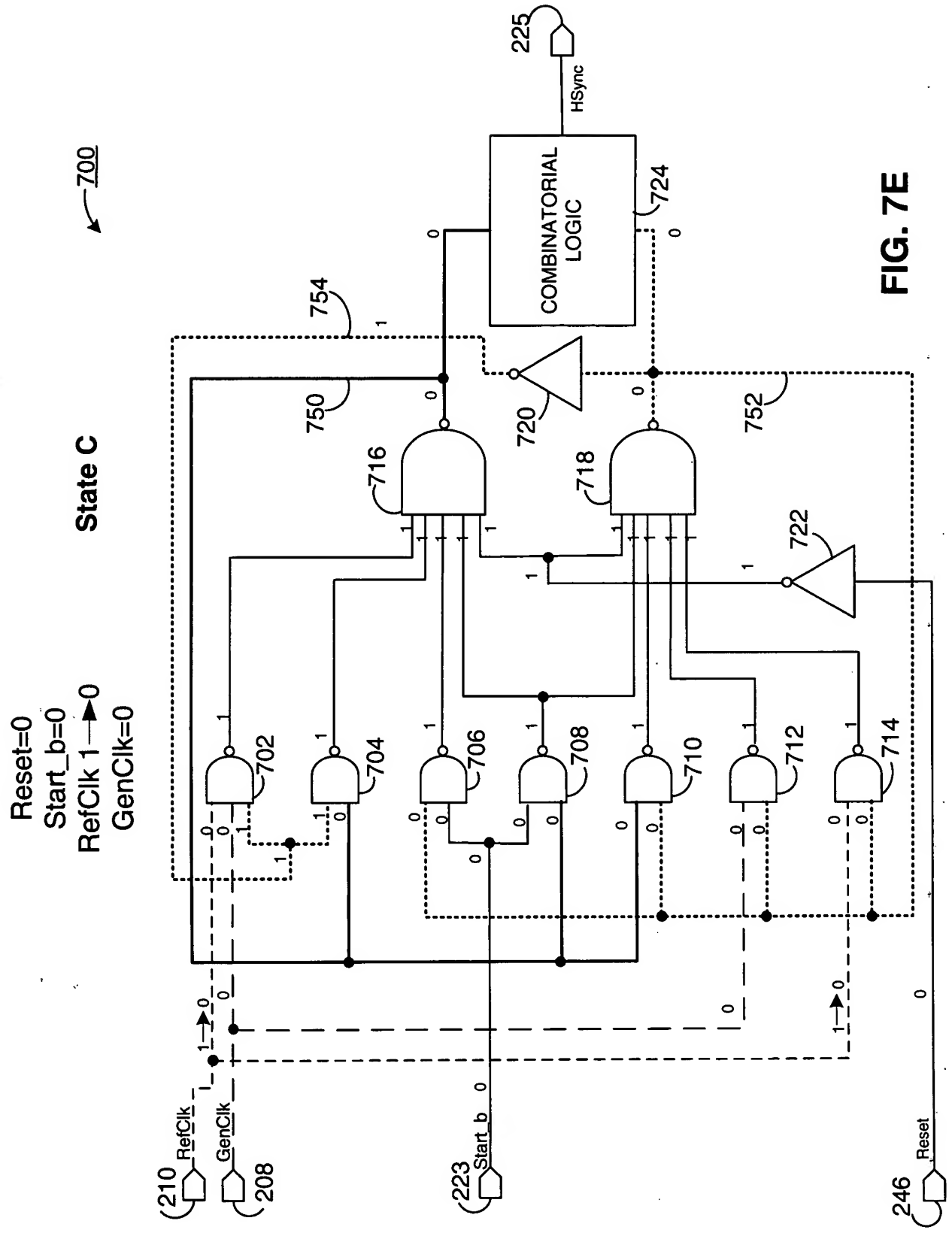
700
State C
Reset=0
Start_b=0
RefClk 1→0
GenClk=0
COMBINATORIAL LOGIC
HSync
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
RefClk
GenClk
Start_b
Reset
210
208
223
246

FIG. 7E

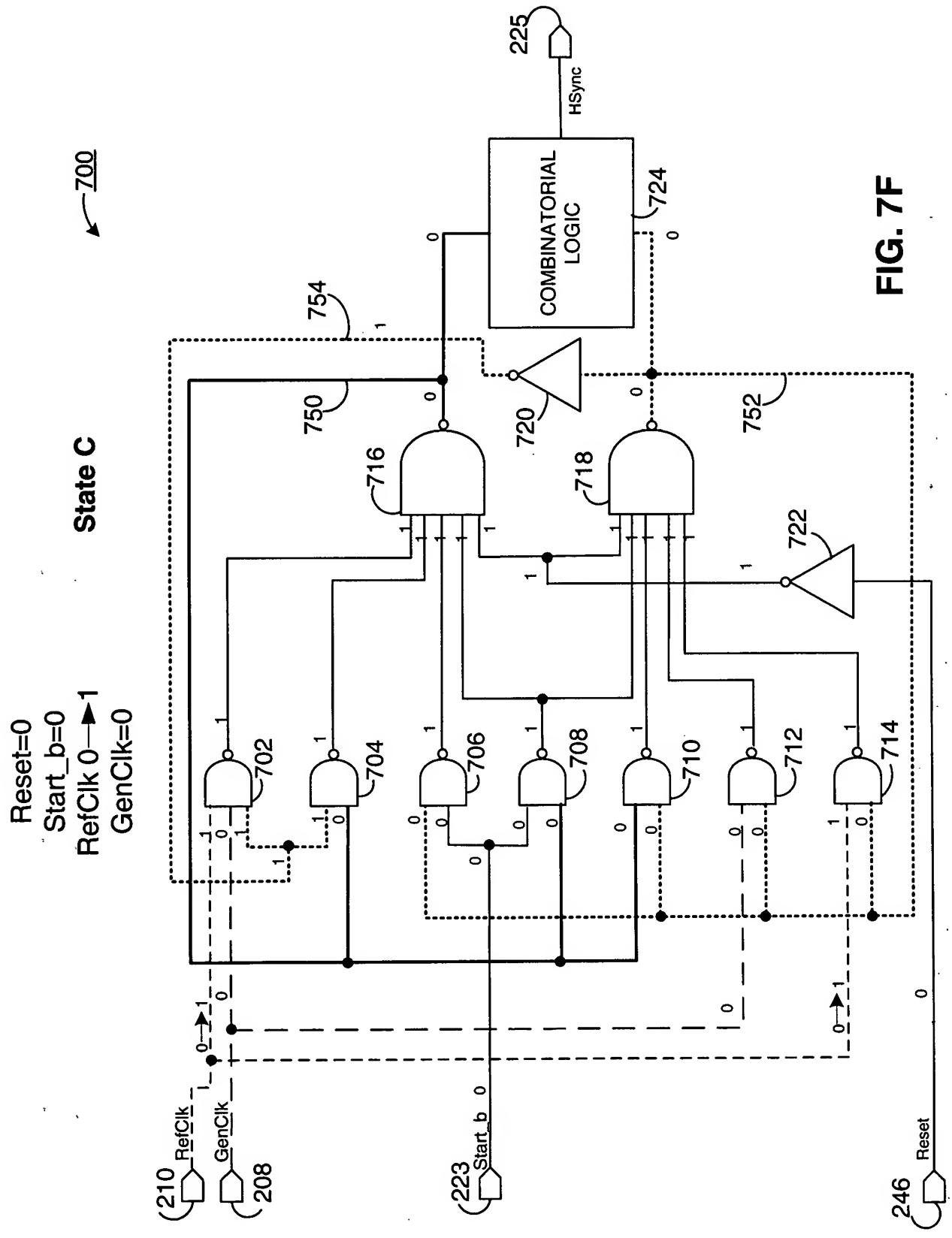
700
State C
Reset=0
Start_b=0
RefClk 0→1
GenClk=0
COMBINATORIAL LOGIC
HSync
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
210
RefClk
208
GenClk
223
Start_b
246
Reset

FIG. 7F

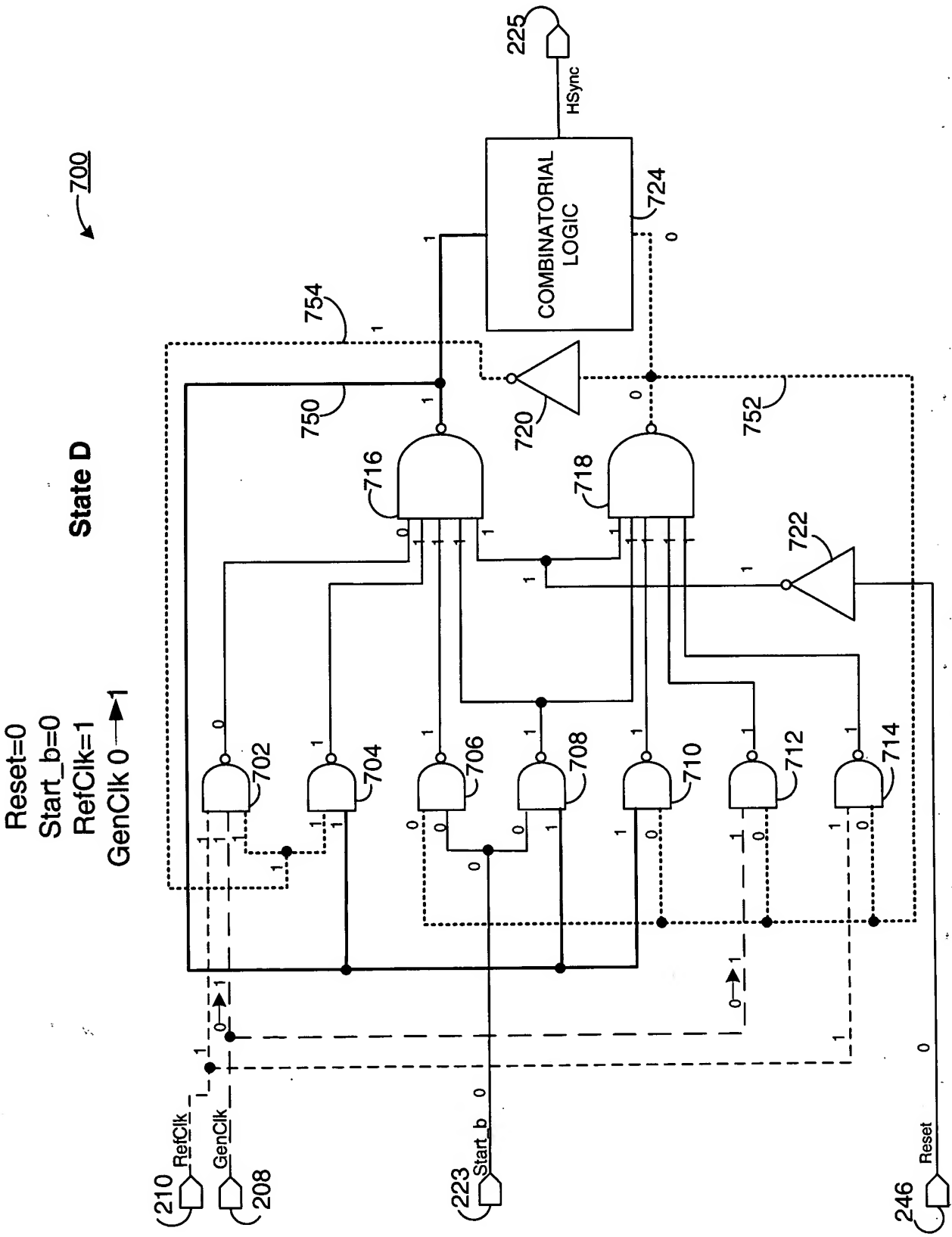
700
State D
Reset=0
Start_b=0
RefClk=1
GenClk 0→1
COMBINATORIAL LOGIC
HSync
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
RefClk
GenClk
Start_b
Reset
210
208
223
246

FIG. 7G

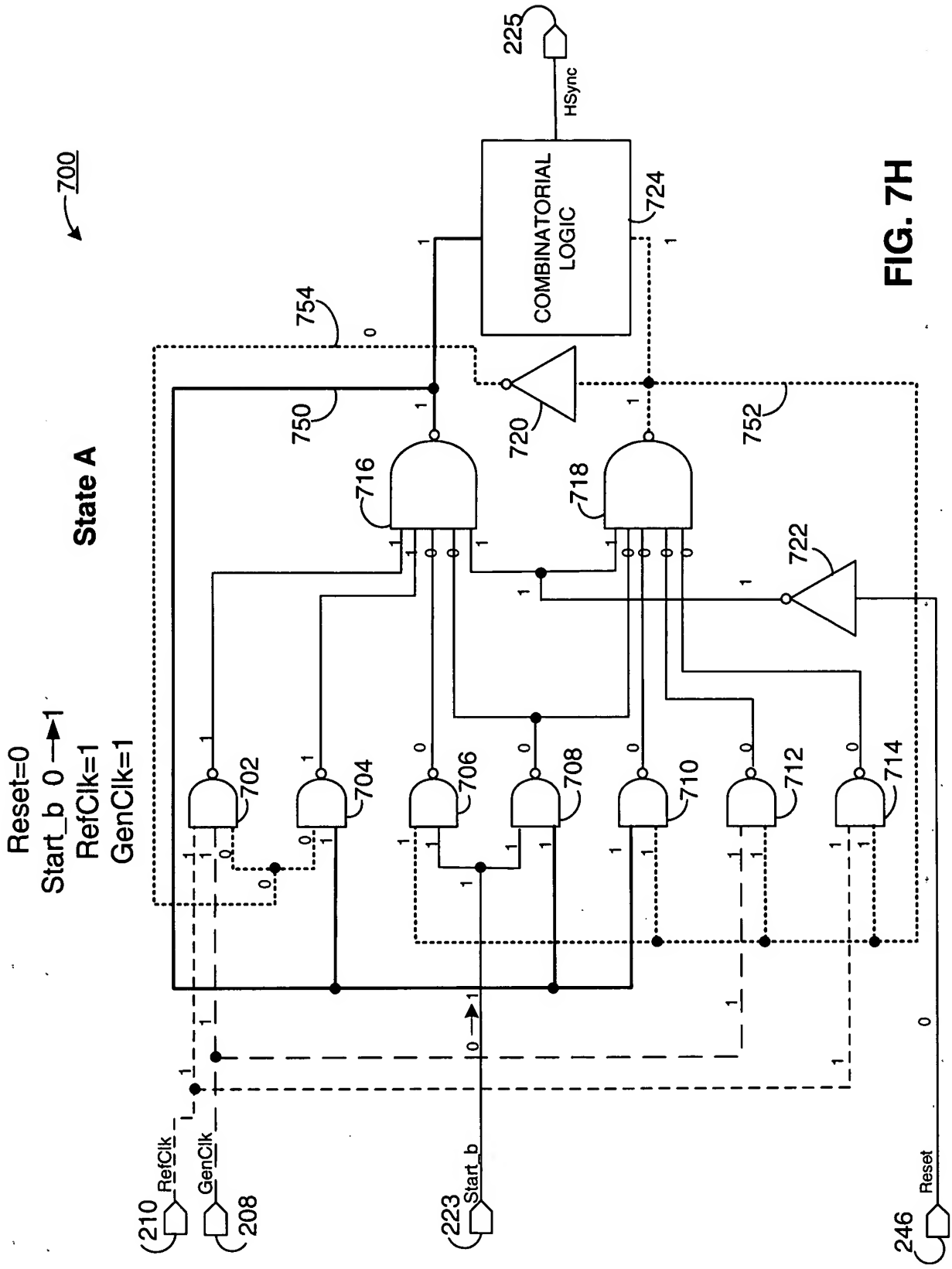
700
State A
Reset=0
Start_b 0→1
RefClk=1
GenClk=1
COMBINATORIAL LOGIC
HSync
225
724
754
750
752
720
716
718
722
702
704
706
708
710
712
714
210
RefClk
208
GenClk
223
Start_b
246
Reset

FIG. 7H

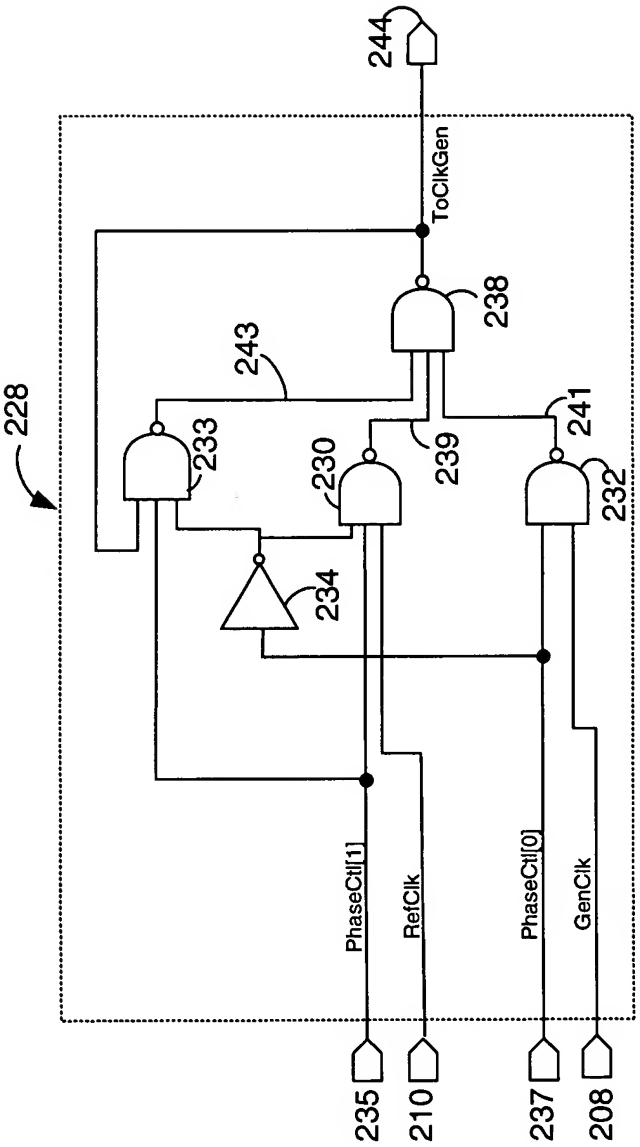
228
244
ToClkGen
238
243
241
233
230
239
232
234
PhaseCtl[1]
RefClk
PhaseCtl[0]
GenClk
235
210
237
208

FIG. 8

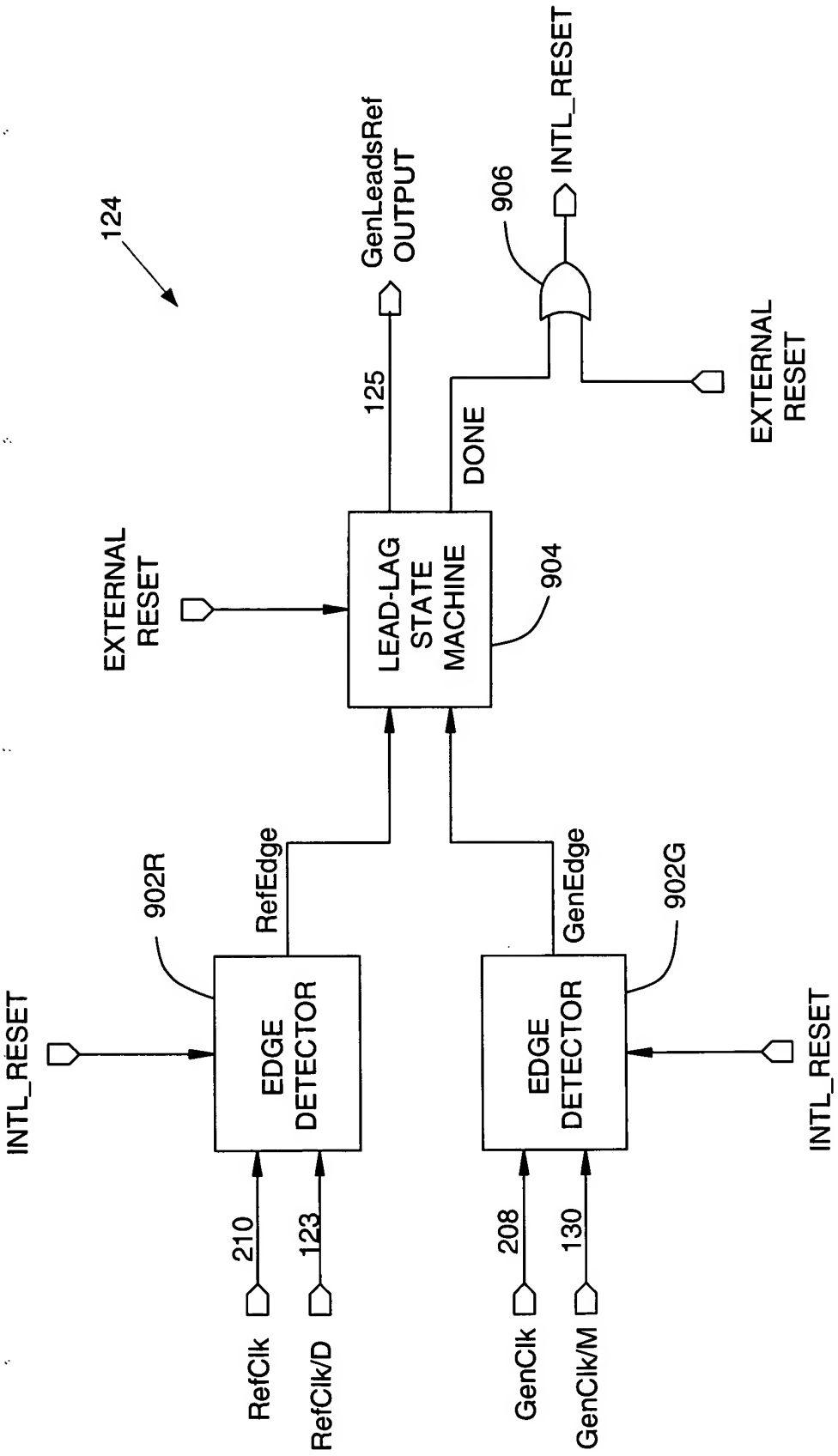
124
GenLeadsRef OUTPUT
125
906
INTL_RESET
EXTERNAL RESET
DONE
EXTERNAL RESET
LEAD-LAG STATE MACHINE
904
902R
RefEdge
GenEdge
902G
INTL_RESET
EDGE DETECTOR
EDGE DETECTOR
INTL_RESET
210
123
208
130
RefClk
RefClk/D
GenClk
GenClk/M

FIG. 9

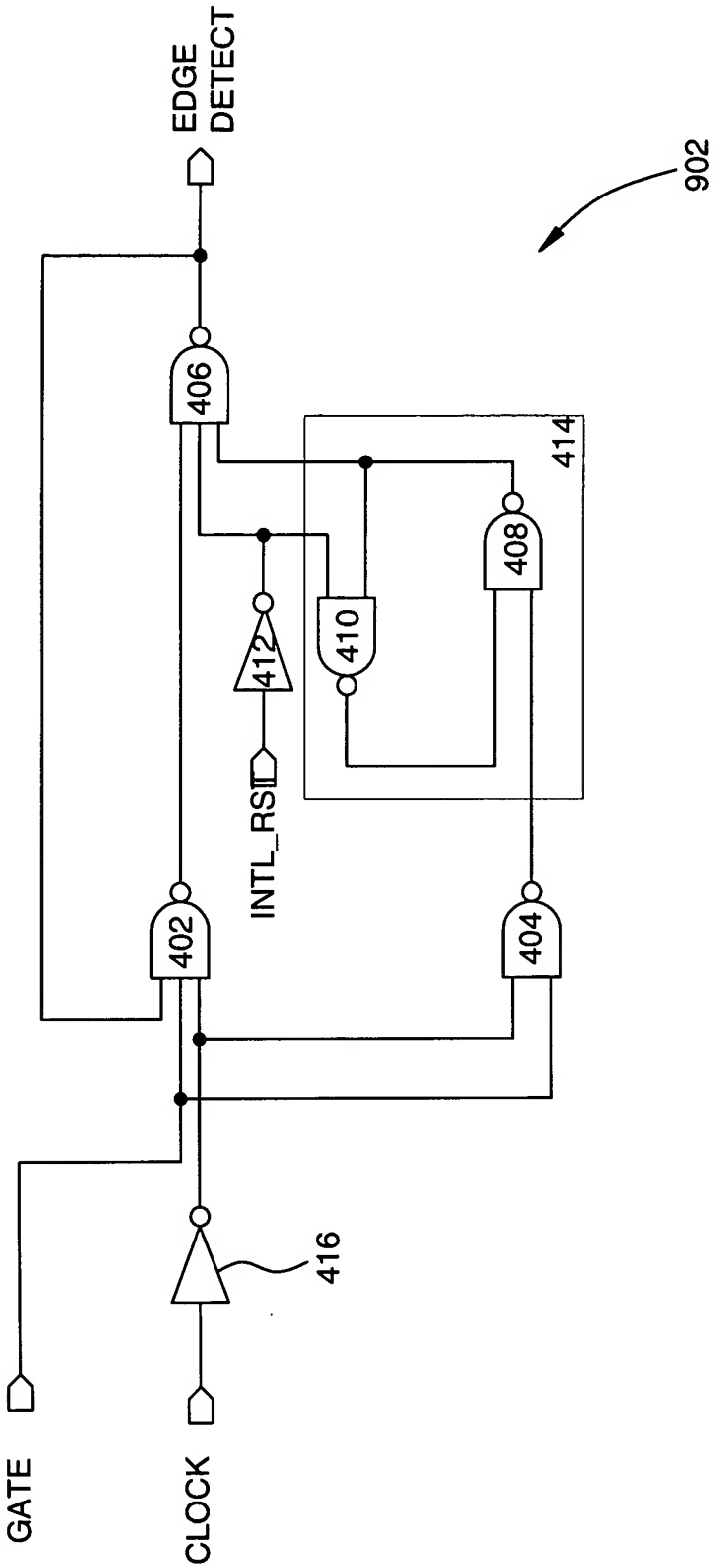
EDGE DETECT
902
406
414
408
410
412
INTL_RST
402
404
416
GATE
CLOCK

FIG. 10

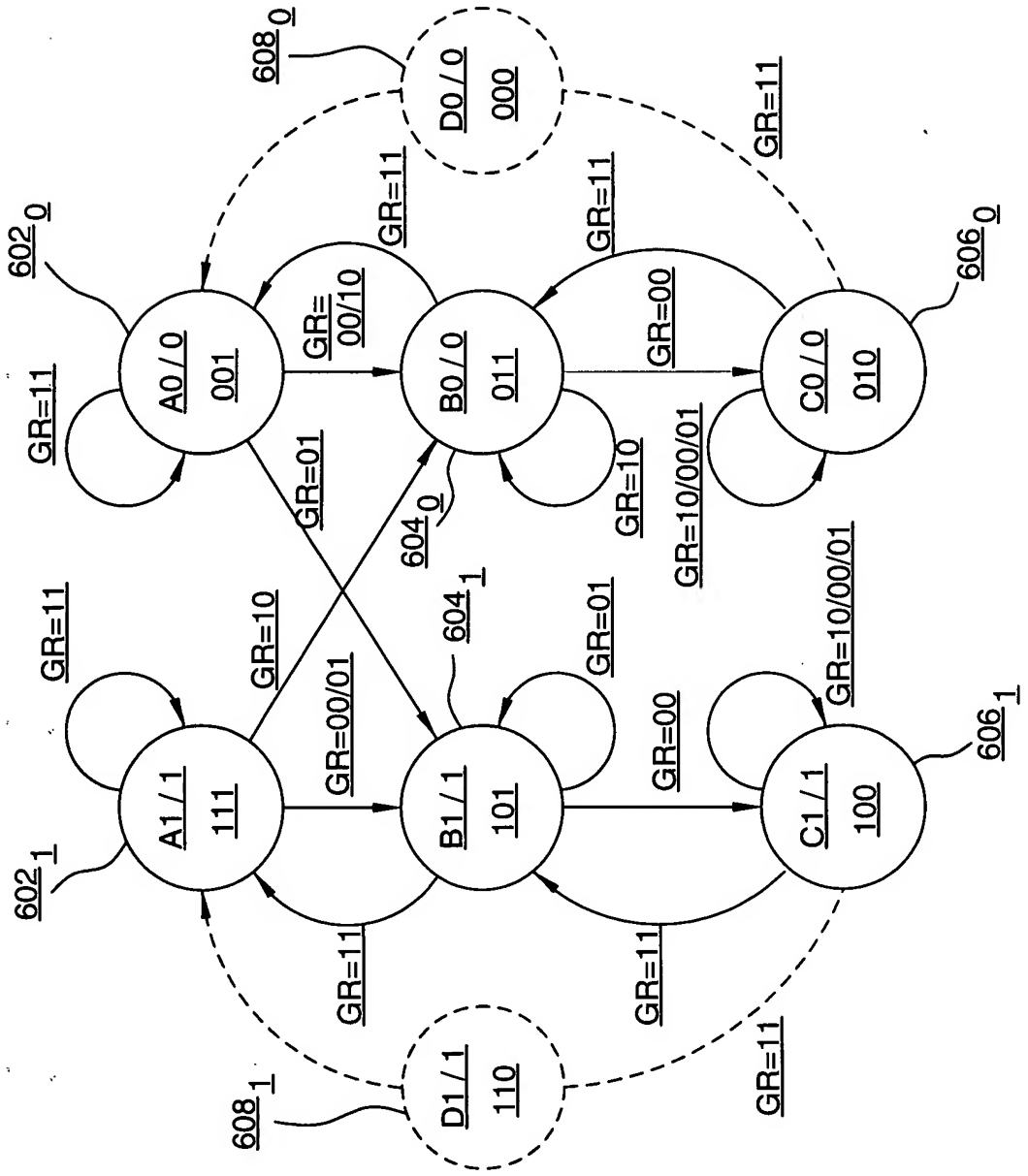
608 0
D0 / 0
000
602 0
A0 / 0
001
B0 / 0
011
C0 / 0
010
606 0
GR=11
GR=11
GR=11
GR=11
GR=
00/10
GR=00
GR=01
GR=10
GR=10/00/01
604 0
604 1
GR=11
GR=10
GR=01
GR=01
GR=00/01
GR=00
GR=10/00/01
602 1
A1 / 1
111
B1 / 1
101
C1 / 1
100
606 1
GR=11
GR=11
GR=11
608 1
D1 / 1
110

FIG. 11

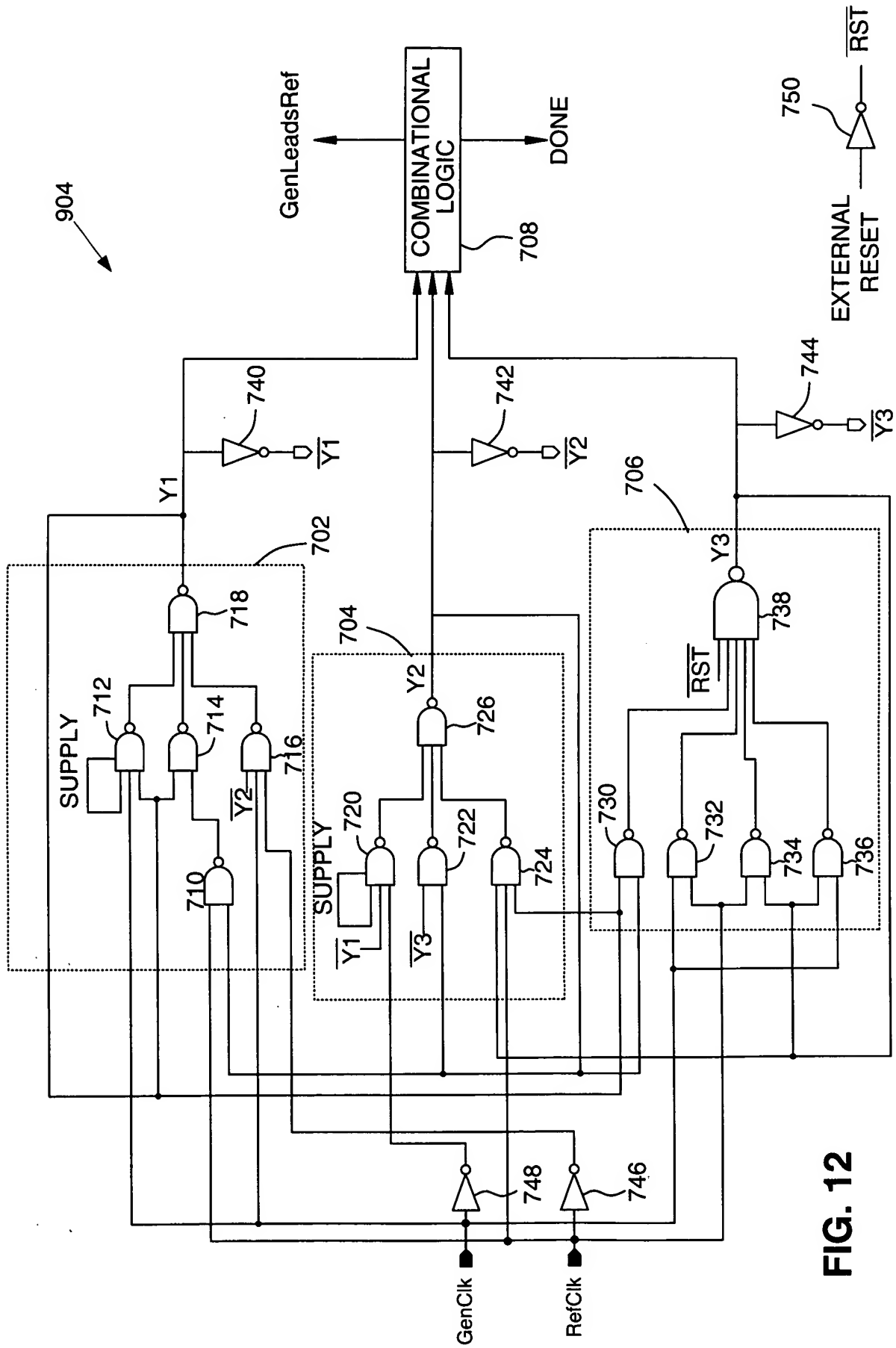
904
GenLeadsRef
COMBINATIONAL LOGIC
708
DONE
750
RST
EXTERNAL RESET
740
742
744
Y1
Y2
Y3
706
702
704
718
738
726
712
714
716
SUPPLY
720
722
724
730
732
734
736
710
748
746
GenClk
RefClk

FIG. 12

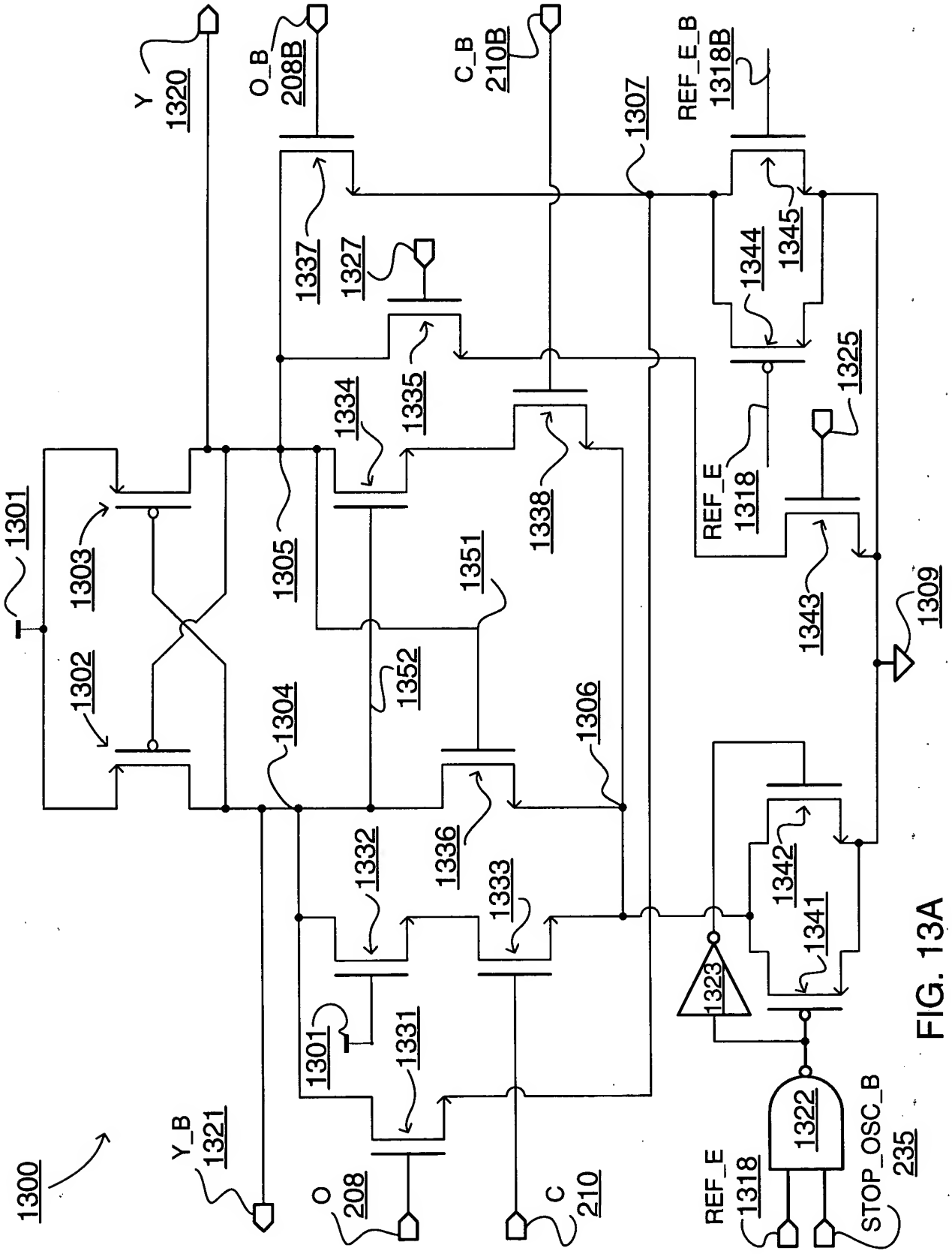
1300
1301
1302
1303
1304
1305
1306
1307
1309
1318
1320
1321
1322
1323
1325
1327
1331
1332
1333
1334
1335
1336
1337
1338
1341
1342
1343
1344
1345
1351
1352
208
210
235
208B
210B
1318B
Y
Y_B
O
C
O_B
C_B
REF_E
REF_E_B
STOP_OSC_B

FIG. 13A

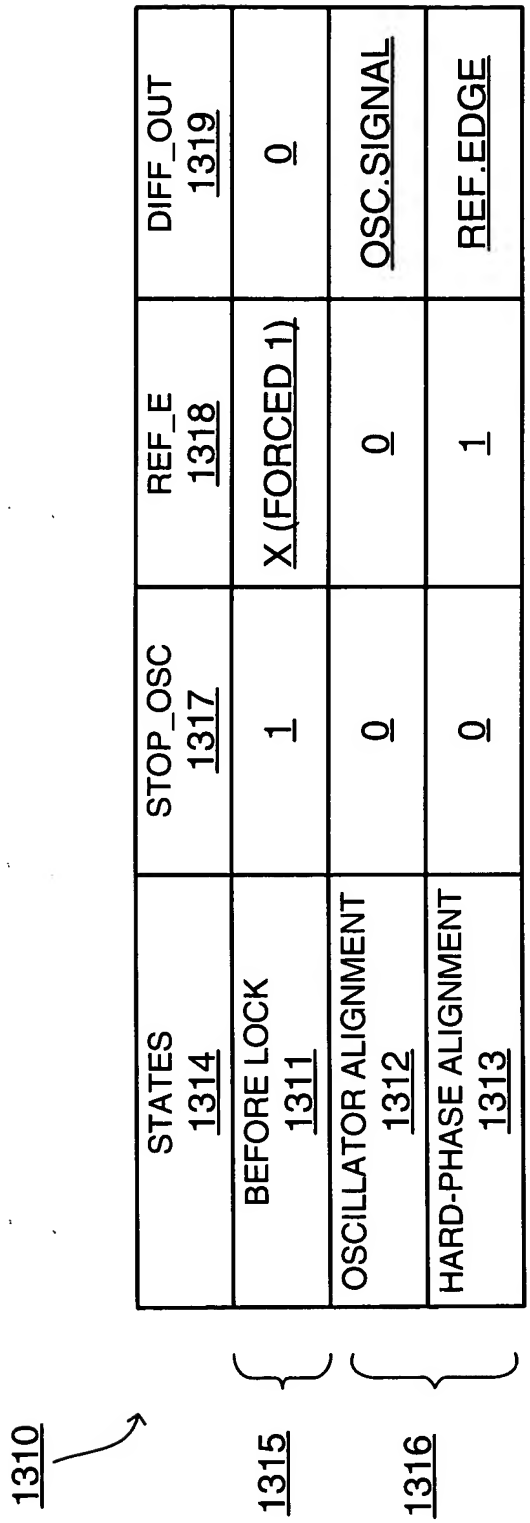


FIG. 13B

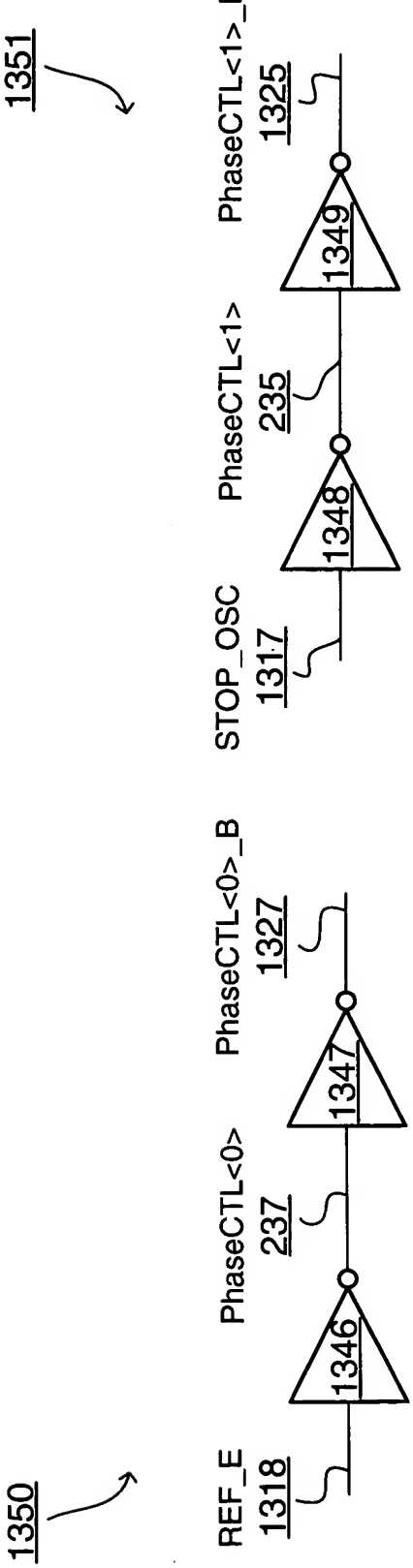


FIG. 13C

FIG. 13D

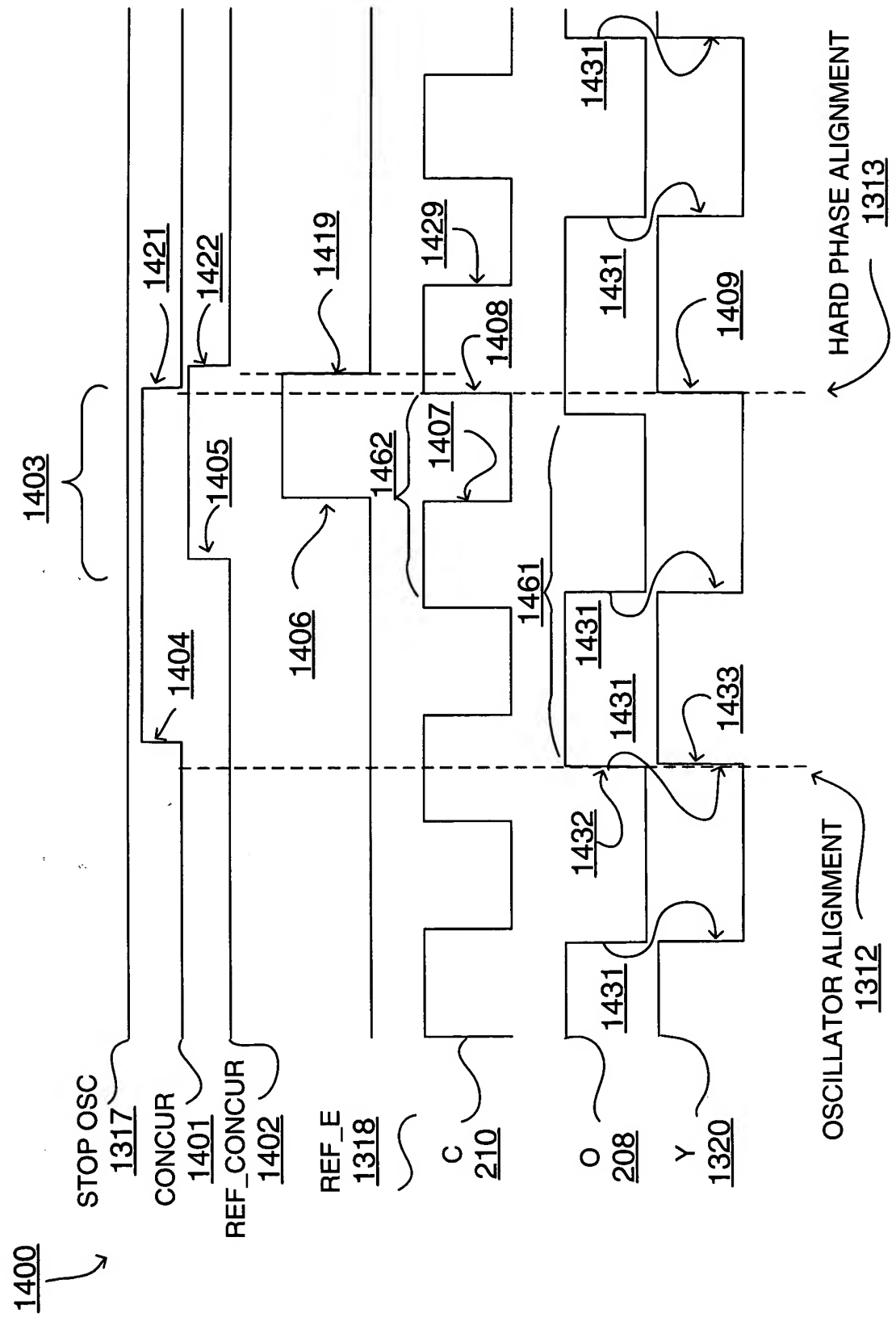
1400
STOP OSC 1317
CONCUR 1401
REF_CONCUR 1402
REF_E 1318
C 210
O 208
Y 1320
OSCILLATOR ALIGNMENT 1312
HARD PHASE ALIGNMENT 1313
1403
1404
1405
1406
1407
1408
1409
1419
1421
1422
1429
1431
1432
1433
1461
1462

FIG. 14

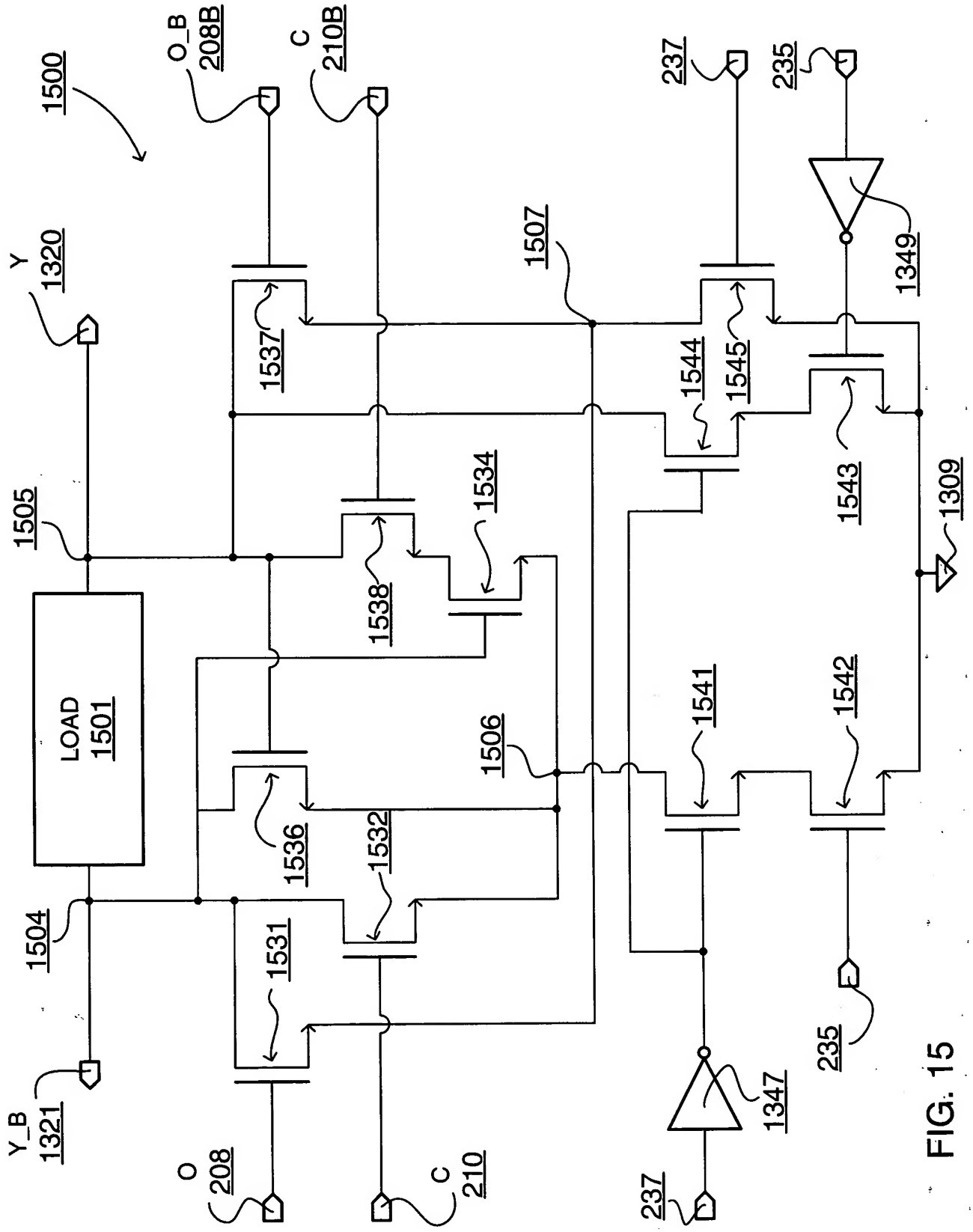
1500
O_B
208B
C
210B
237
235
Y
1320
1507
1349
1537
1544
1545
1505
1534
1543
1309
1538
LOAD
1501
1506
1541
1542
1536
1532
1504
1531
Y_B
1321
O
208
C
210
237
1347
235

FIG. 15

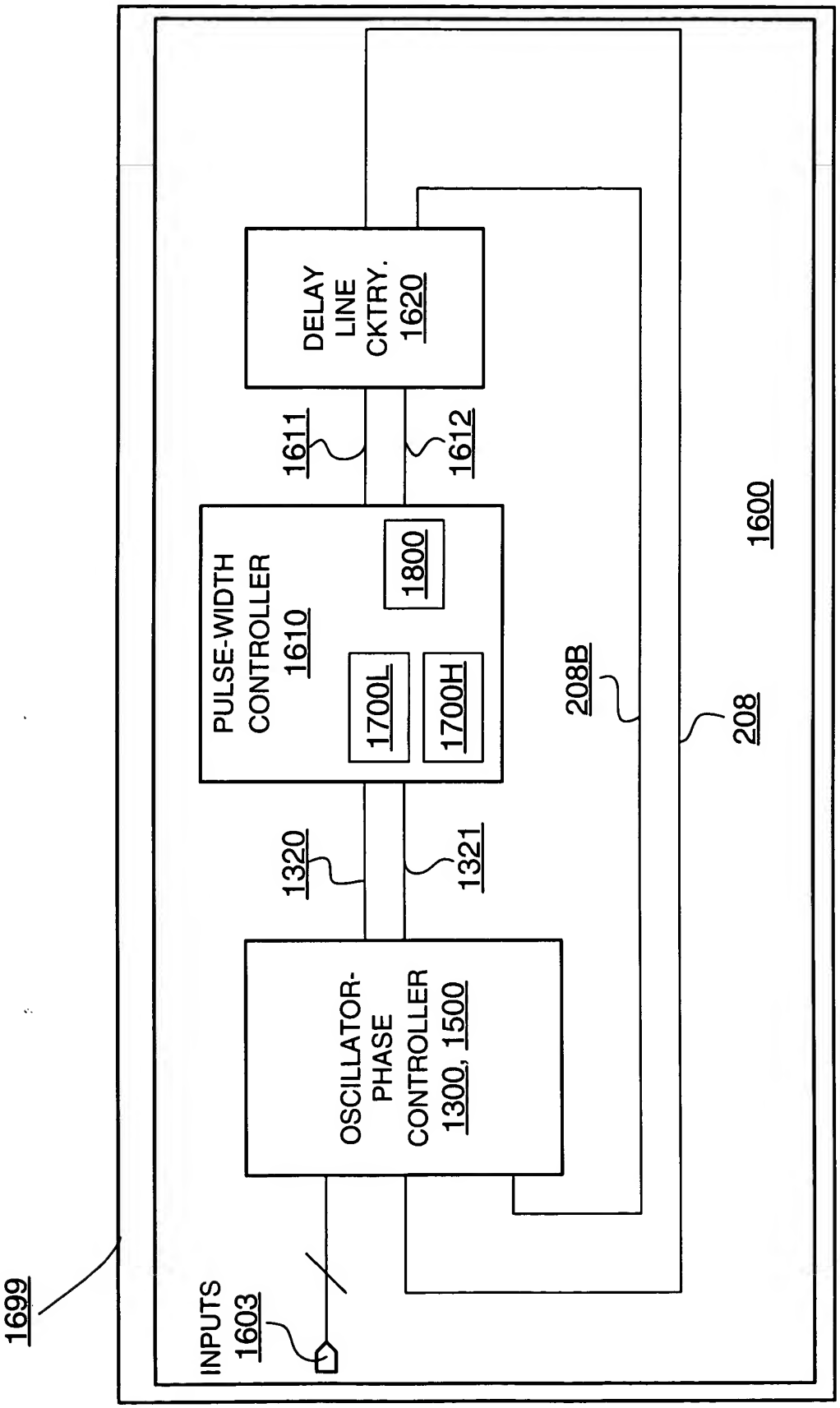
1699
INPUTS
1603
OSCILLATOR-PHASE CONTROLLER 1300, 1500
1320
1321
PULSE-WIDTH CONTROLLER 1610
1700L
1700H
1800
DELAY LINE CKTRY. 1620
1611
1612
208B
208
1600

FIG. 16

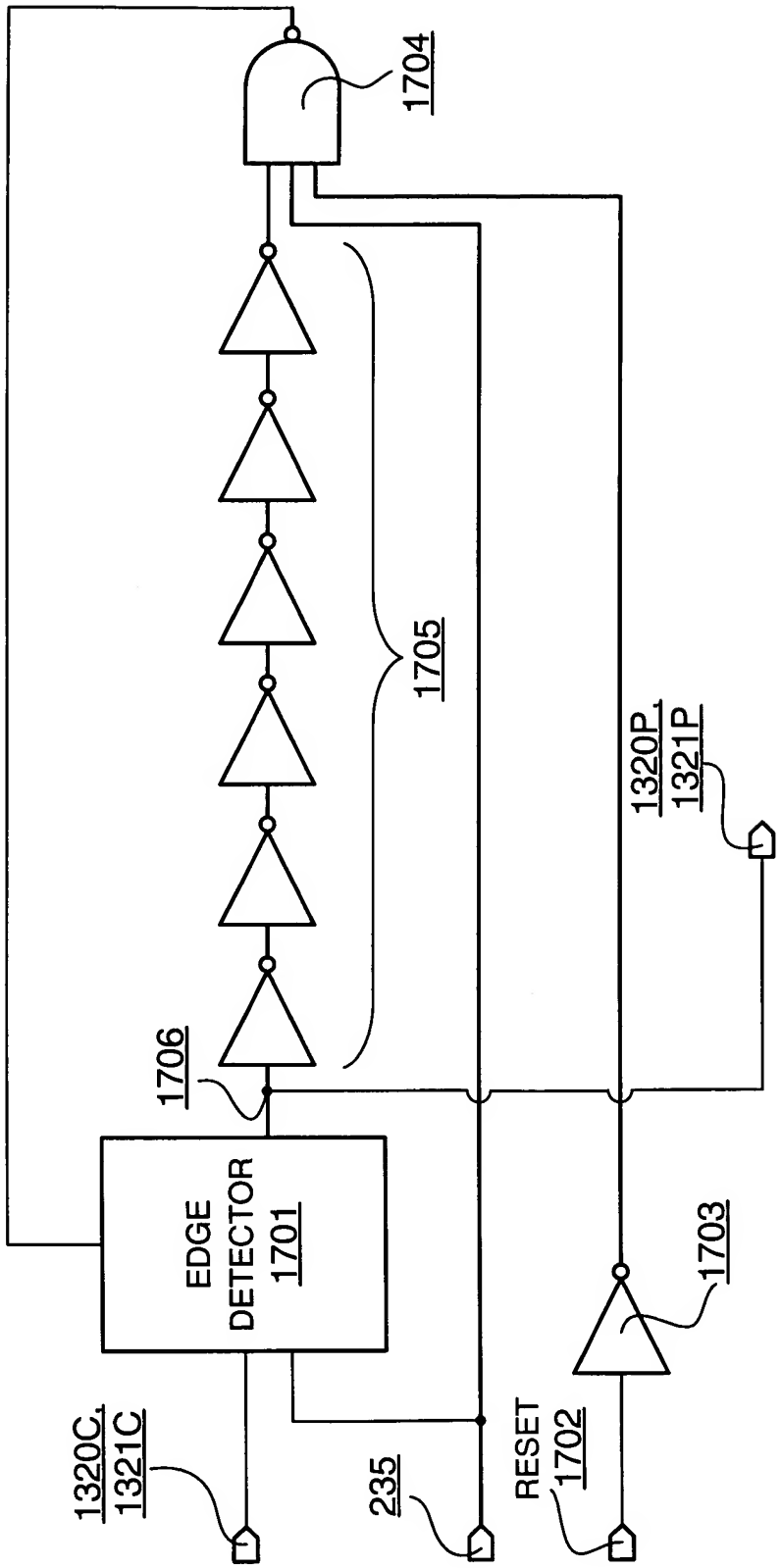
1704
1705
1706
EDGE DETECTOR 1701
1320C, 1321C
235
RESET 1702
1703
1320P, 1321P
1700

FIG. 17

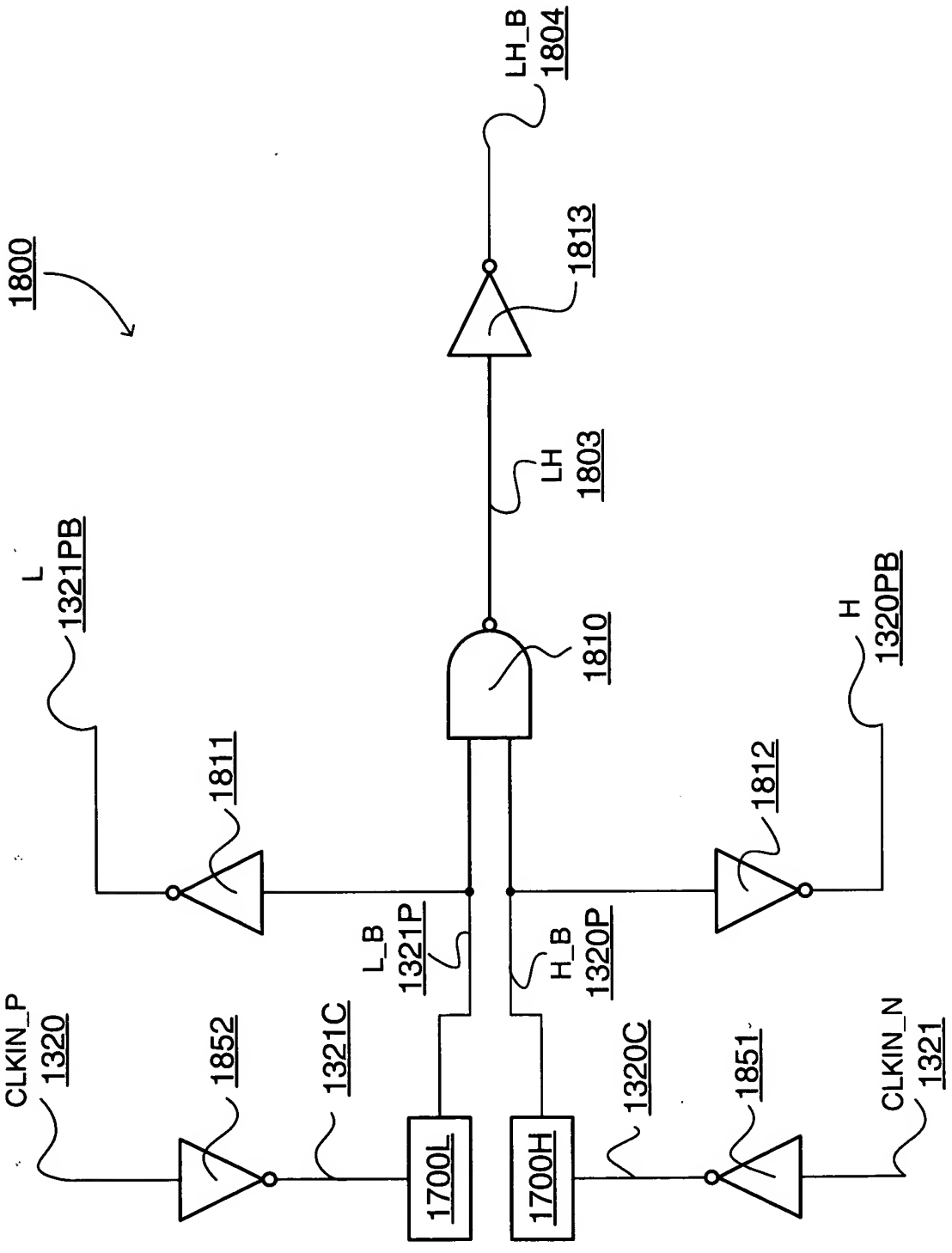
1800
LH_B
1804
1813
LH
1803
L
1321PB
1810
H
1320PB
1811
1812
L_B
1321P
H_B
1320P
CLKIN_P
1320
1852
1321C
1700L
1700H
1320C
1851
CLKIN_N
1321

FIG. 18A

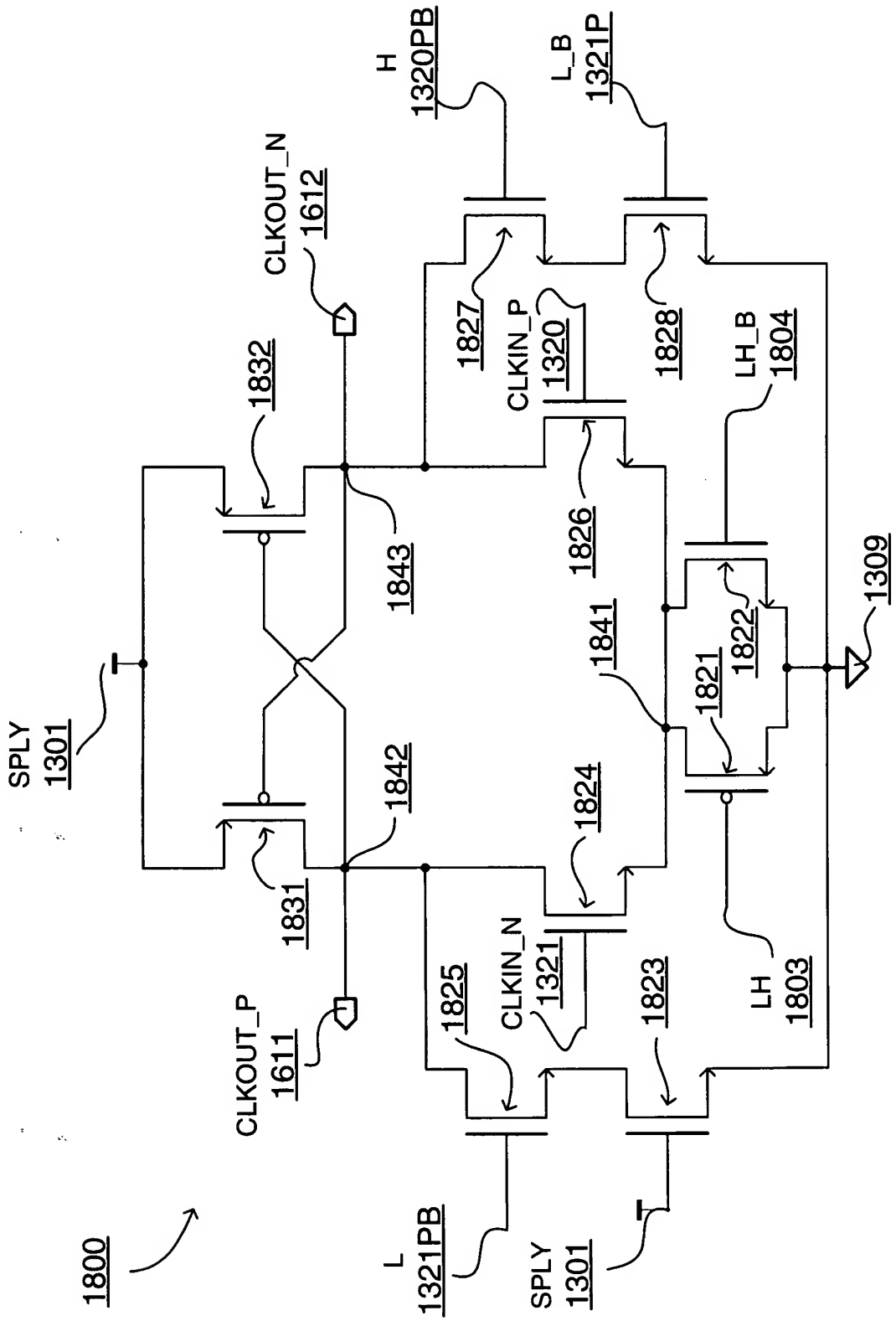
1800
SPLY
1301
CLKOUT_P
1611
CLKOUT_N
1612
L
1321PB
H
1320PB
L_B
1321P
SPLY
1301
LH
1803
LH_B
1804
1309
1831
1832
1842
1843
1824
1825
1826
1827
1828
1841
1821
1822
1823
CLKIN_N
1321
CLKIN_P
1320

FIG. 18B

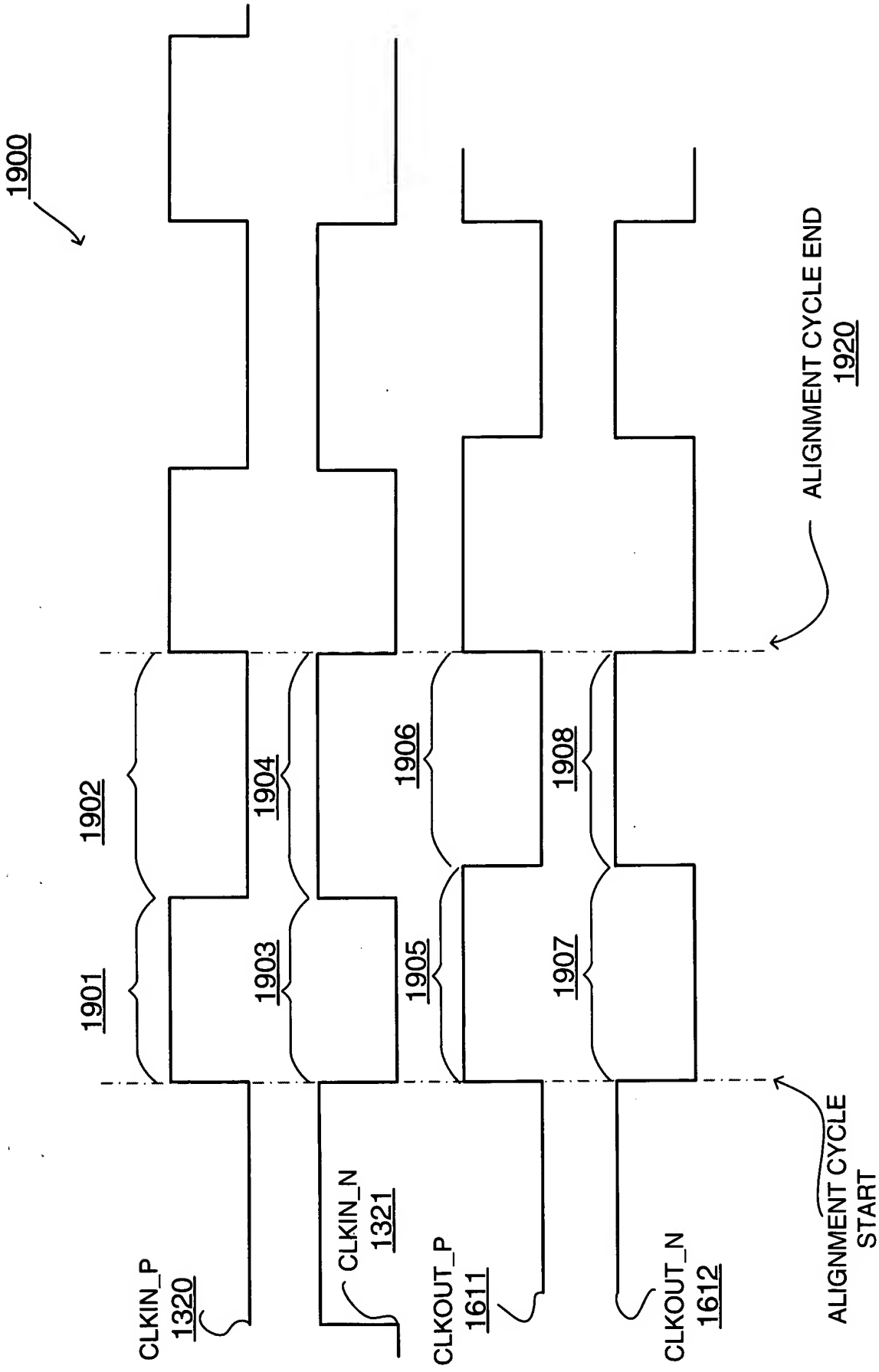
1900
1901
1902
1903
1904
1905
1906
1907
1908
CLKIN_P
1320
CLKIN_N
1321
CLKOUT_P
1611
CLKOUT_N
1612
ALIGNMENT CYCLE START
1910
ALIGNMENT CYCLE END
1920

FIG. 19